

Review of Lab 0 & DE0-Nano Intro

EE 231L

KEY CONCEPTS

- If you are unsure of something:
 - Datasheet
 - TA/Instructor
 - Lab Attendant
- Purpose of these labs:
 - Lab 0
 - Build a clock source
 - Gain experience with wire wrapping
 - Lab 1
 - Utilize the clock source
 - Recognize gate delays & implications thereto

Lab 0

Utilizes 4 basic components:

- 74HC4040
- 74HC14
- Oscillator
- LED & resistor
- Key realizations
 - COLOR CODE EVERYTHING
 - Position parts properly
 - Proper wire wrapping skills
 - How to use documentation

IC Basics

- There is ALWAYS an indicator for Pin 1
 - Dot
 - Notch
 - Edge
 - Stripe
 - http://www.evilmadscientist.com/2010/basicsfinding-pin-1/
- Pin counting is ALWAYS CCW
- Diagrams are ALWAYS top down views

74HC4040

- $Q0 = clk/2^{1}$
- $Q1 = clk/2^2$
- $Q2 = clk/2^3$
- Etc...



74HC14

Inverting buffers with Schmitt trigger





Table 3.	Function table ^[1]	
Input	Output	
nA	nY	
L	Н	
Н	L	

[1] H = HIGH voltage level;L = LOW voltage level.



D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
1	EOH	Enable Input or No Connect
7 or 4	GND	Circuit & Package Ground
8 or 5	Output	RF Output
14 or 8	V _{cc}	Supply Voltage



Wiring Diagram:



Ground:





Pin 3 - LED and Slow Output:



Where is the clock?

Clock:



Dividers:



Clock Rates:

- 4 jumper selected rates:
 - 2^0 Jumper 4–5
 - 2^4 Jumper 3–6
 - 2^8 Jumper 2–7
 - 2^12 Jumper 1–8
- 5 additional division rates per jumper:
 - 2^5 Pin 8
 - 2^6 Pin 7
 - 2^7 Pin 6
 - 2^8 Pin 5
 - 2^9 Pin 4
 - 2^10 Pin 3
- > 20 total clock rates

DE0-Nano

- Cyclone IV FPGA
- SDRAM
- 8 channel A/D
- 3 axis Accelerometer



Figure 1-1 The DE0-Nano Board

DE0-Nano





Figure 3-3 Connections between the push-buttons and Cyclone IV FPGA



Figure 3-4 Pushbuttons debouncing

DEO-Nano

