Electrical Engineering
New Mexico Institute of Mining and Technology

EE 231L – Fall 2014

Laboratory Syllabus

Instructor / TAs

Dr. Hector Erives – Course Instructor

- Email: erives@ee.nmt.edu
- Office Hours: M-F 1000-1100
  Tuesday 1400-1700
  Wednesday 1400-1700

Jordan Keeley – Lead TA

- Email: jkeeley@nmt.edu
- Office Hours: W 1700-2100

Ryan Schwingle – Lead TA

- Email: rschwing@nmt.edu
- Office Hours: M 1700-2100

Maya Robinson – Assistant TA

Additional office hours are available upon request.

Topics / Learning Objectives

In this course, one will explore Boolean logic, logic gates, and Verilog programming. One will also implement advanced digital systems, such as memory and arithmetic logic units using an FPGA and Verilog.

Grading

Pre-laboratory exercise:	30%
Laboratory exercise:	
Format:	20%
Introduction:	10%
Procedure:	30%
Conclusion:	10%
Total:	**100%**

Table 1: Grading Rubric

Late/Sick Policy

Uncoordinated absences will result in a zero for that lab grade. Email your lead TA with information about planned absences; if necessary, also contact the Dean of Students (Melissa Jaramillo-Fleming) for the appropriate paperwork.

Students are expected to attend lab at the scheduled time. Tardiness of more than 30 minutes will result in a grade penalty of 50% on your prelab.

Lab books are due 2 days after the student's assigned lab section, by 1700. Late lab books will be docked 10% per day.

Make-Up Policy

There will be one formal make-up week at the end of the semester, wherein students may submit a missed lab for full credit. Improving one's grade can be accomplished by writing and turning in a formal report in IEEE format for that lab within two weeks of said laboratory, for up to 90% credit.

Lab Book and Formal Report Expectations

Laboratory notebooks shall have an introduction detailing the learning objective of each lab and any background information necessary to understand the contents thereof. Following the introduction, the detailed procedure should be noted clearly, including all observations, data, and analysis. All figures should be labeled and referenced in the text. Finally, a conclusion shall be present to bring the lab full circle, summarizing the expectations and realizations of the lab in question. Even unsuccessful labs can receive a grade of 100% if and only if the notebook documents what failed, why, and how it could be improved.

Formal reports are to be written in IEEE format, must be at least 3 pages long, and will be due within 2 weeks of the lab if they are used as a grade-improvement tool. The final project will have a formal report (worth 2 lab grades), which will be due by 1700 on December 5, 2014. No work will be accepted after this deadline.

Safety

When working with live electronics, soldering irons, or other laboratory equipment, students are required to wear their safety goggles.

Counseling & Disability

Counseling services are available at Tech for students carrying 6 or more credit hours, free of charge. If you happen to have a disability, please visit the OCDS office in Fidel to ensure appropriate accommodations are made. For more information, visit the office, call 575-835-6619, or email counseling@admin.nmt.edu.

Academic Honesty and FERPA

Working with a partner in lab is allowed and in some cases encouraged. However, all lab notebooks and formal reports will be individual efforts. Plagiarism will not be tolerated. Review the NMT Academic Honesty Policy.
Grades are available upon request. Lab notebooks will be returned in person during normal class hours (generally on Monday), in compliance with FERPA as an additional layer of protection for all students.

Emergencies

In an emergency, call Campus Police at 575-835-5555 or dial 911 and specify your location.

Tentative Lab Schedule

Tuesday	Wednesday	Number	Title
08/26/14	08/27/14	Lab 0	Wire Wrapping Project: Counter Board
09/02/14	09/03/14	Lab 1	HCMOS Logic Family
09/09/14	09/10/14	Lab 2	Introduction to Verilog HDL and Quartus
09/16/14	09/17/14	Lab 3	Decoders and Multiplexers
09/23/14	09/24/14	Lab 4	Debouncing Switches
09/30/14	10/01/14	Lab 5	4-Bit Adder/Subtractor
10/07/14	10/08/14	Lab 6	Arithmetic Logic Unit
10/14/14	10/15/14	Lab 7	Sequential Circuits
10/21/14	10/22/14	Lab 8	Registers
10/28/14	10/29/14	Lab 9	Computer control Unit
11/04/14	11/05/14	Lab 9	Computer control Unit
11/11/14	11/12/14	Lab 10	Build a Computer
11/18/14	11/19/14		Make-up week