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Lab 0: HCMOS Logic Family

Introduction

In this lab you will get a hands-on experience designing simple logic circuits using standard integrated circuits (ICs). You will learn about timing and its effect on the circuit output.

1.Prelab
1.1.Write the truth table for an *inverter* gate.
1.2.Write the truth table for a 2-input *xor* gate.
1.3.Write the truth table for a 2-input *and* gate.
1.4.Write the truth table for the circuit shown in Figure 1. (Hint: What happens with an even number of inverters? How about odd?)
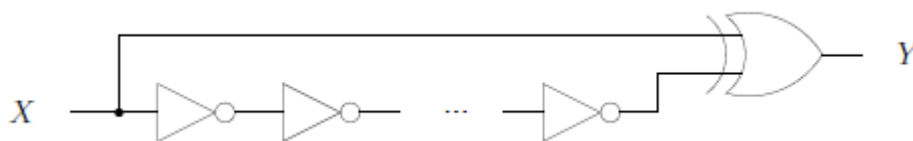

Figure 1: A simple circuit

1.5 For the following logic statement, create a K-map.
$$f(x_1,x_2,x_3) = x_1 x_2 x_3 + x_1' x_2 x_3 + x_1 x_2 x_3' + x_1 x_2' x_3' + x_1' x_2' x_3'$$

1.6 Simplify the equation using the K-map technique.

2. Lab

2.1 Basic Behavior of HCMOS Logic Family

2.1.1   Use the datasheet to connect a 7404 IC.

2.1.2 Connect the input to GND and check that the output is a logic 1 using the logic probe. After, connect the input to V_{CC} of 5 V and check that the output is now a logic 0.

2.1.3 Use a variable 10kΩ potentiometer to vary the input to the inverter, as shown in Figure 1. The potentiometer will be the blue one with the white knob on top. The knob will only turn around 2/3 of a full rotation and is used for coarse adjustments. **When does the input change?**
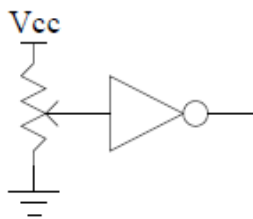
Figure 1: Changing the input to the inverter

2.1.4 Build the circuit shown in Figure1 below using 10 inverters in series. Using the protoboard, set the function generator to 100 KHz. **Can you observe the output of your circuit by using a voltmeter or a logic probe?**

2.1.5 Connect the output of your circuit to the logic analyzer and record your observations. (Use the information provided in section 3 to run the logic analyzer).

2.1.6 Does the output match what you expected? Why or why not?

2.1.7 What is the propagation delay of an inverter gate?

2.2 Half Adder

2.1 **Write the truth table for the circuit shown in Figure 3.**

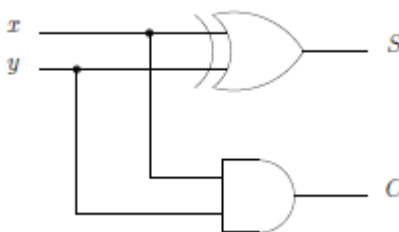2.2 Connect ICs from the 7400 IC to implement the circuit shown below.

Figure 3: Half Adder Circuit

2.3 Verify that operation of the circuit by connecting the inputs to different combinations of Vcc and GND.

2.4 **In terms of binary arithmetic, what do the S and C outputs represent?**

3 Supplementary Material: Logic Analyzer

3.1 Start the logic analyzer by double-clicking on the LA Viewer icon on the Windows desktop. Do the following:

- From the Clock menu in the upper right corner of the LA Viewer window set the internal clock for a 5 MHz sampling rate.

- Right-click in the left most column of the viewing area and select delete all labels.

- Right-click in the left most column of the viewing area and select add label. Add representative names and select the appropriate channels.

- Click on play button neat the top of the window. The logic analyzer will sample the logic levels on lines 0 and 1.

3.2 Observe the Waveform window. You can use the Magnifying Glass icons on the menu bar to zoom in and out. **Does the waveform make sense to you?** Print a sample of the waveform, and put it in your lab notebook. To print a copy of this waveform, make sure the logic analyzer software is in the foreground (it is the current program). Then, press Alt+PrtScn to take a snapshot of that window. You can now paste this image into Word which will make it easy to print out.

3.3 Another way of displaying logic data is as numbers. Right-click on the leftmost column, select combine labels, give this label any name, move all labels from source box to destination box where output is at the top, and the is at the bottom and click OK. Right click on that name, select Configure Labels, and Change Group Type to binary. **How does this numeric data compare to a truth table format?**

3.4 NOTE: *LA Viewer* is not a perfect program. Connect the logic analyzer to the PC before starting the program. If it starts in "demo mode" it failed to detect, and you need to reconnect the logic analyzer and restart the program.

3.5 NOTE: *LA Viewer* is not a prefrect program. Disconnecting the logic analyzer or pulling the USB calb e will cause the program to auto-exit. Please save your work frequently. DO NOT WAIT UNTIL THE END TO PRINT YOUR RESULTS.