Homework \#2 Due September 19, 2007
3.1 Consider the circuit shown in Fig. P3.1.
a) Show the truth table for the logic circuit $f$.
b) If each gate in the circuit is implemented as a CMOS gate, how many transistors are needed?


Fig. P3.1. A sum-of-products CMOS circuit.
3.2 a) Show that the circuit in Fig. P3.2 is functionally equivalent to the circuit in Fig. P3.1.
b) How many transistors are needed to build this CMOS circuit/


Fig. P3.2. A CMOS circuit built with multiplexers.
3.7 a) Give the truth table for the CMOS circuit in Fig. P3.5.
b) Derive the simplest sum-of-products expression for the truth table in part (a). How many transistors are needed to build the sum-of-products circuit using CMOS AND, OR, and NOT gates?


Fig. P3.5. A four-input CMOS circuit.
3.8 Fig. P3.6 shows half of a CMOS circuit. Derive the other half that contains the PMOS transistors.


Fig. P3.6. The PDN in a CMOS circuit.
3.11 Derive a CMOS complex gate for the logic function $f\left(x_{1}, x_{2}, x_{3}, x_{4}\right)=\sum m(0,1,2,4,6,8,10,12,14)$.
3.19 For a PMOS transistor, assume that $\mathrm{k}^{\prime}{ }_{\mathrm{p}}=16 \mu \mathrm{~A} / \mathrm{V}^{2}, \mathrm{~W} / \mathrm{L}=3.5 \mu \mathrm{~m} / 0.35 \mu \mathrm{~m}, \mathrm{~V}_{\mathrm{GS}}$ $=-3.3 \mathrm{~V}$, and $\mathrm{V}_{\mathrm{T}}=-0.66 \mathrm{~V}$. For $\mathrm{V}_{\mathrm{DS}}=-3.2 \mathrm{~V}$, calculate $\mathrm{R}_{\mathrm{DS}}$.
3.30 Repeat problem 3.29 for the parameters $\mathrm{k}_{{ }_{\mathrm{n}}}=40 \mu \mathrm{~A} / \mathrm{V}^{2}, \mathrm{k}_{\mathrm{p}}{ }_{\mathrm{p}}=0.4 \times \mathrm{k}_{\mathrm{n}}, \mathrm{W}_{\mathrm{n}} / \mathrm{L}_{\mathrm{n}}=$ $\mathrm{W}_{\mathrm{p}} / \mathrm{L}_{\mathrm{p}}=3.5 \mu \mathrm{~m} / 0.35 \mu \mathrm{~m}, \mathrm{~V}_{\mathrm{DD}}=3.3 \mathrm{~V}$.
3.46 Given the function $f=x_{1} x_{2} x_{3}+x_{2} x_{3} \bar{x}_{4}+\bar{x}_{1} \bar{x}_{2} \bar{x}_{3}$, a straightforward implementation in an FPGA with three-input LUTs requires four LUTs. Show how it can be done using only 3 three-input LUTs. Label the output of each LUT with an expression representing the logic function that it implements.
3.50 Assume that a gate array exists in which the logic cell used is a three-input NAND gate. The inputs to each NAND gate can be connected to either 1 or 0 , or to any logic signal. Show how the following logic functions can be realized in the gate array (Hint: use DeMorgan's theorem.)
a) $f=x_{1} x_{2}+x_{3}$
b) $f=x_{1} x_{2} x_{4}+x_{2} x_{3} \bar{x}_{4}+\bar{x}_{1}$

