Homework \#5 Due November 19, 2007
4.10 Derive a minimum-cost realization of the four variable function that is equal to 1 if exactly tow or exactly three of its variables are equal to 1 ; otherwise it is equal to 0 .
4.21 Find the minimum-cost circuit for the function $\mathrm{f}(\mathrm{x} 1, \ldots, \mathrm{x} 4)=\Sigma \mathrm{m}(0,4,8,13,14,15)$. Assume that the input variables are available in uncomplemented form only. (Hint: use functional decomposition).
4.23 Use the tabular method discussed in section 4.9 to find a minimum cost SOP realization for the function $\mathrm{f}(\mathrm{x} 1, \ldots, \mathrm{x} 4)=\Sigma \mathrm{m}(0,2,4,5,7,8,9,15)$.
4.33 Consider the circuit in Figure P4.2, which implements functions $f$ and $g$. What is the cost of this circuit, assuming that the input variables are available in both true and complemented forms? Redesign the circuit to implement the same functions, but at as low a cost as possible. What is the cost of your circuit?


Figure P4.2. Circuit for problem 4.33.
6.1 Show how the function $\mathrm{f}(\mathrm{w} 1, \mathrm{w} 2, \mathrm{w} 3)=\Sigma \mathrm{m}(0,2,3,4,5,7)$ can be implemented using a 3-to- 8 binary decoder and an OR gate.
6.4 Repeat problem 6.3 for the function $f=\overline{w 2} \overline{w 3}+w 1 w 2$.
6.7 Consider the function $f=\overline{w 2}+\overline{w 1} \overline{w 3}+w 1 w 3$. Show how repeated application of Shannon's expansion can be used to derive the minterms of f .
6.11 Consider the function $f=\overline{w 1} \overline{w 2}+\overline{w 2} \overline{w 3}+w 1 w 2 w 3$. Give a circuit that implements $f$ using the minimal number of two-input LUTs. Show the truth table implemented inside each LUT.
6.31 Figure 6.21 shows a block diagram of a ROM. A circuit that implements a small ROM, with four rows and four columns, is depicted in Figure P6.3. Each X in the figure represents a switch that determines whether the ROM produces a 1 or 0 when that location is read.


Figure P6.3. A $4 \times 4$ ROM circuit.
(a) Show how a switch (X) can be realized using a single NMOS transistor.
(b) Draw the complete $4 \times 4$ ROM circuit, using your switches from part (a). The ROM should be programmed to store the bits 0101 in row 0 (top row), 1010 in row 1,1100 in row 2 , and 0011 in row 3 (bottom row).

