# EE 231 – Homework Chapter 6

**6.1** Show how the function $f(w_1, w_2, w_3) = \sum m(0,2,3,4,5,7)$ can be implemented using a 3-to-8 binary decoder and an OR gate.

**6.6** For the function $f(w_1, w_2, w_3) = \sum m(0,4,6,7)$ use Shannon's expansion to derive an implementation using a 2-to-1 multiplexer and any other necessary gates.

**6.9** Prove Shannon's expansion theorem presented in section 6.1.2. Hint: use perfect induction, i.e. prove the theorem by showing that the expression for every possible value of $x_i$.

**6.16** Actel Corporation manufactures an FPGA family called Act 1, which has the multiplexer-based logic block illustrated in Figure P6.1. Show how the function $f = w_2\overline{w}_3 + w_1w_3 + \overline{w}_2w_3$ can be implemented using only one Act 1 logic block.

**6.19** Write Verilog code that represents the function in problem 6.2, using a **case** statement.

**6.22** Figure P6.3 shows a modified version of the code for a 2-to-4 decoder in Figure 6.42. This code is almost correct but contains one error. What is the error?

**6.28** Write Verilog code that represents the circuit in Figure 6.19. Use the dec2to4 module in figure 6.35 as a subcircuit in your code.

**6.32** Show the complete circuit for a ROM using the storage cells designed in Part (a) of problem 6.31 that realizes the logic functions:

$$d_3 = a_0 \oplus a_1, \quad d_2 = \overline{a_0 \oplus a_1}, \quad d_1 = a_0a_1, \quad d_0 = a_0 + a_1$$