Name_____

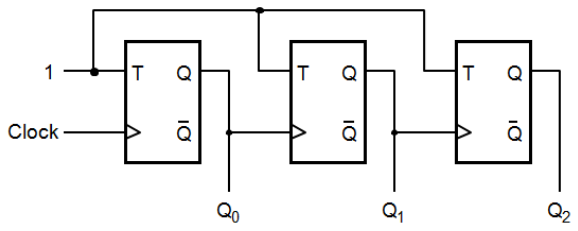
Partial credit will be given if you show your work.

1. (25 pts.) For the function $f(w_1, w_2, w_3) = \sum m(0,2,3,6)$, use Shannon's expansion to derive an implementation using a 2-to-1 multiplexer and any other necessary gates.

2. (25 pts.) An SR flip-flop is a flip-flop that has set and reset inputs like a gated SR latch (as shown in its characteristic table). Show how an SR flip-flop can be constructed using a D flip-flop and other logic gates.

S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	0

3. (25 pts.) The figure below shows the implementation of a three-bit counter with T Flip-Flops. What is the sequence that the circuit counts in (assume that Q_0=Q_1=Q_2=0 at t_0)?



4. (25 pts.) The following control circuit is used to control a three-register computer system through a multiplexed Bus. A partially completed timing diagram shows the contents of the registers before an operation is initiated. Complete the timing diagram, showing the contents of the Bus and registers (in Hexadecimal).