EE231 STUDY GUIDE - Exam 1

Chapter 2 – Introduction to Logic Circuits

Variables and Functions:

Series connections of switches implement AND functions
Parallel connections of switches implement OR functions

Truth tables:

Basic operations can be defined in the form of a table.

Logic gates and networks:

ANDs, ORs, NOTs, BUFFERS (TRI-STATE BUFFERS), XORs, NANDs, NORs.

Timing diagrams:

Show waveforms at the output when the inputs change through time.

Functionally equivalent networks:

A logic function can be implemented with different networks (possibly different costs).

Boolean algebra:

Axioms, theorems, two and three-variable properties: commutative, distributive, absorption, combining, and DeMorgan's.

Venn diagrams:

Simple visual way that is used to verify theorems, properties, and functions.

Synthesis using AND, OR, and NOT gates:

Starting with a truth table we can synthesize a circuit or find the function.

Sum-Of-Products (SOP) and Product-Of-Sums (POS):

Can use minterms and maxterms to synthesize circuits.

Multiplexer circuits

Used to select different input to a circuit.

Chapter 3 – Implementation Technology

Voltage levels:

VDD, V1,min, V0,max, VSS (Gnd).

Transistor switches:

NMOS, PMOS.

CMOS logic gates:

Defined by a Pull-Down Network (PDN) that involves NMOS transistors ONLY, and a Pull-Up Network (PUN) that involves PMOS transistors ONLY.

CMOS gates:

They are formed by switching on/off transistors in the PDN and the PUN (transistors act as switches in SERIES and/or PARALLEL.
NOT, AND, OR, NAND, NOR, …

Field-Programmable Gate Arrays (FPGAs):

Internal connections that include logic, I/O, interconnections blocks.
The logic blocks are implemented with LUTs, and multiplexers are used to select specific storage cells from the LUTs.

Practical aspects of MOSFET fabrication and behavior:

Current in the transistor, I_D , depends on TRIODE or SATURATION region.
The transistor on resistance, R_{DS}.
The current in steady-state, I_{STAT}.

Dynamic operation of logic gates

Parasitic capacitance.
Propagation delay, t_p.

Power consumed in steady state

$P_S = I_{STAT} \times V_{DD}$

Power consumed dynamically

$P_D = f \times C \times V_{DD}^2$

Fan-In

The maximum number of inputs to a gate.

Fan-out

The maximum number of gates, a gate can drive.

EE231 STUDY GUIDE - Exam 2

Chapter 4 – Implementation of Logic Functions

Karnaugh Maps:

2-variable, 3-variable, and 4-variable maps (5-variable maps will not be included in the test because by nature they are lengthy procedures to be included in a 1-hour test).

Cost of implementation:

A Karnaugh map can produce more than one implementation, but with different costs. We want to select the less expensive implementation.

Minimization of POS forms:

Use minterms to find a minimum implementation.

Minimization of SOP forms:

Use maxterms to find a minimum implementation.

Incompletely specified functions:

Functions that contain DON'T CARE conditions can be used to our advantage to minimize a function.

Multiple output circuits:

When sub-functions are repeated in the implementation of two or more functions, terms can be shared to minimize cost.

Multilevel synthesis:

Multilevel functions can be synthesized el functions on FPGAs through the use of look-up tables or LUTs.

Functional decomposition:

A complex circuit can be decomposed into much simpler sub-circuits by assigning variable names to strategic points within the circuit.

Chapter 5 – Number Representation and Arithmetic Circuits

Signed and unsigned integers:

-Digital systems use binary representations or base-2.

-Right-most bit is the LSB, left-most bit is the MSB.

Conversion between decimal & binary systems:

-Conversion from decimal to binary is found by dividing successively by 2.

-Conversion from binary to decimal is found by multiplying by 2 each binary value.

Important radices in computer systems:

Binary, octal, and Hex (short for hexadecimal).

Half Adder (HA) and Full Adder (FA):

-HAs are used to add/subtract one bit.

-FAs are used to add/subtract one than one bit (FA are formed by groups of HA).

Ripple-Carry adder:

Each FA in the ripple-carry adder introduces a delay. The delay is proportional to the number of bits being added.

Signed number representation:

-Sign and magnitude, 1's complement, and 2's complement.

Addition and subtraction:

1's complement addition, 2's complement addition.

Arithmetic overflow:

Used to indicate that a summation/subtraction can't be expressed using a specific number of bits.

Carry-Lookahead adder:

The delay in a carry-lookahead adder is fixed (at the expense of increasing circuit complexity).

Multiplication:

Is carried out the same way we do it when we multiply decimal numbers.

Other number representations:

The BCD (binary coded decimal) is used to represent the standard 10 digits (0-9) in binary.

EE231 STUDY GUIDE - Exam 3 and Chapter 8

Chapter 6 – Implementation of Logic Functions

Multiplexers:
- Implementation in FPGAS through programmable switches.

Synthesis of logic functions using multiplexers.

Multiplexer synthesis using Shannon's Expansion.

Shannon's Expansion Theorem.

Decoders, and demultiplexers

Encoders:
- Binary encoders.

Code converters.

Arithmetic Logic Unit (ALU).

Chapter 7 – Flip-flops, registers, counters, and a simple processor

Basic latch

Gated SR latch

Gated D latch

Effects of propagation delays

Master-slave and edge-triggered D flip-flops

D , T, and JK flip-flops.

Registers.
- Shift register.

Counters:
- Synchronous.
- Asynchronous.
- Parallel-access shift register.

Reset synchronization.

BCD counter.

Design examples: Bus Structure, Simple Processor.

Chapter 8 – Synchronous sequential circuit

Basic design steps.

State diagram.

State stable.

State assignment.

Choice of flip-flops, and derivation of next-state and output expressions.
Timing diagram.

Design steps for an FSM.
    Bus implementation example.

State assignment problem.

Moore and Mealy state models.

Serial adder example:
    Mealy-type
    Moore-type

State minimization: Partitioning minimization procedure.

Design of counters using the sequential circuit approach.