Review for Exam III

Analog/Digital Converters

• Methods used for A/D converters
  – Flash (Parallel)
  – Successive Approximation

• A/D converters are classified according to:
  – Resolution (number of bits)
  – Speed (number of samples per second)

• The MC9S12 has two 10-bit successive approximation A/D converters - can be used in 8-bit mode

• The MC9S12 uses an analog multiplexer to allow eight input pins to connect to any of the A/D converters

• The quantization level of the A/D converter

$$\Delta V = (V_{RH} - V_{RL})/2^b$$

• There are inputs on the HCS12 for the reference voltages V_{RL} and V_{RH}
  – In normal operation $V_{RL} = 0$ V and $V_{RH} = 5$ V.
  – You must have $V_{SS} \le V_{RL} < V_{RH} \le V_{DD}$.

• Register that need to use to set up the A/D subsystem:

ATD1CTL2 ATD1CTL3 ATD1CTL4 ATD1CTL5	Control Regs

ATD1STAT0	Status Reg

The MC9S12 IIC Interface

• The IIC bus can control multiple devices using only two wires
  – The two wires are Clock and Data
  – The lines are normally high. Any device on the bus can bring them low.

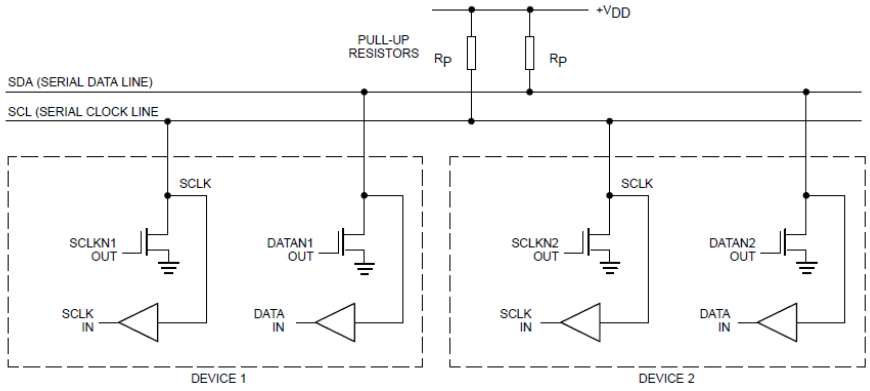
• Each device on the bus has a unique address

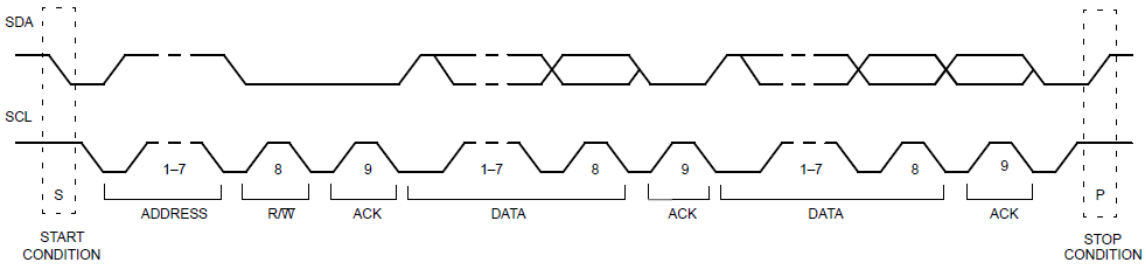
• An IIC master starts the process by sending out a serial stream with the seven-bit address of the slave it wants to talk to, and an eighth bit indicating if it wants to write to the slave or read from the slave

• If it writes to the slave, it will continue to send data on the serial data line until all the data is sent.

• If it reads from the slave, it will release the data line, and activate the clock line. The slave takes over the data line, and sends out its data in response to the clock provided by the master.

• After all of the data is transferred, the master releases both the clock and the data lines



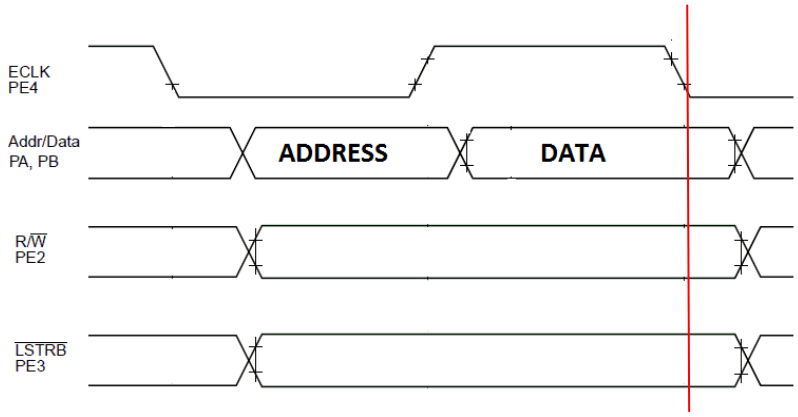


A complete data transfer

The MC9S12 in Expanded Mode

- MC9S12 uses Ports A and B as mulitplexed address/data bus
  In expanded mode, you can no longer use Ports A and B for I/O

- 16–bit Bus:
  While E low, bus supplies address (from MC9S12)
  While E high, bus supplies data (from MC9S12 on write,
  From memory on read)



- When the MC9S12 writes data to memory:
  1. Puts address on the address bus (when E-clock goes low)
  2. Brings the Read/Write (R/W) line low
  3. Puts the data it wants to write onto the data bus
  4. External device needs to latch the data on falling edge of the E-clock

- When the MC9S12 reads data to memory:
  1. Puts address on the address bus (when E-clock goes low)
  2. Brings the Read/Write (R/W) line high
  3. MC9S12 expects external device to put data on the data bus
  4. External device needs to latch the data on falling edge of the E-clock

$\overline{\text{LSTRB}}$	A0	Type of Access
0	**0**	16-bit access of an even address Accesses bytes at even address and subsequent odd address
0	**1**	8-bit access of an odd address
1	**0**	8-bit access of an even address
1	1	**Not allowed on external bus**

- **The MC9S12 in Expanded Mode – Timing**
- Huang Chapter 14

Using the MC9S12 Expanded Bus — Timing Issues

• In expanded mode, memory and peripherals can be added to the MC9S12.

• In order for the expansion to work, the interface timing must be correct.

• Here we will discuss adding more RAM memory to the MC9S12.

• It is necessary to look at the timing of the MC9S12, the "glue logic" (the chips between the MC9S12 and the memory) and the memory to see if all the specs are met.

• Below we will analyze the timing issues for the external memory, and find out what frequency of MC9S12 bus clock is needed to be able to use the external RAM.

• The RAM we will evaluate is a 55 ns Samsung K6T1008C2E (128Kx8 bit Low Power CMOS Static RAM)

Parameter List		Symbol	Speed Bins				Units
			55ns		70ns		
			Min	Max	Min	Max	
Read	Read Cycle Time	t_{RC}	55	-	70	-	ns
	Address Access Time	t_{AA}	-	55	-	70	ns
	Chip Select to Output	t_{CO}	-	55	-	70	ns
	Output Enable to Valid Output	t_{OE}	-	25	-	35	ns
	Chip Select to Low-Z Output	t_{LZ}	10	-	10	-	ns
	Output Enable to Low-Z Output	t_{OLZ}	5	-	5	-	ns
	Chip Disable to High-Z Output	t_{HZ}	0	20	0	25	ns
	Output Disable to High-Z Output	t_{OHZ}	0	20	0	25	ns
	Output Hold from Address Change	t_{OH}	10	-	10	-	ns
Write	Write Cycle Time	t_{WC}	55	-	70	-	ns
	Chip Select to End of Write	t_{CW}	45	-	60	-	ns
	Address Set-up Time	t_{AS}	0	-	0	-	ns
	Address Valid to End of Write	t_{AW}	45	-	60	-	ns
	Write Pulse Width	t_{WP}	40	-	50	-	ns
	Write Recovery Time	t_{WR}	0	-	0	-	ns
	Write to Output High-Z	t_{WHZ}	0	20	0	25	ns
	Data to Write Time Overlap	t_{DW}	20	-	25	-	ns
	Data Hold from Write Time	t_{DH}	0	-	0	-	ns
	End Write to Output Low-Z	t_{OW}	5	-	5	-	ns

• The interface uses 18 address lines (A17-0). The MC9S12 allows you to use more than 16 address lines by paging the memory. You select a memory page with Port K, and use a CALL and RTC (Return from CALL) instructions to switch pages.

– The **PPAGE** register keeps the page value, which is written to Port K.
It allows up to 256 16kB program memory pages to be switched into and out of the program memory window. This provides up to 4 MB of paged program memory space)

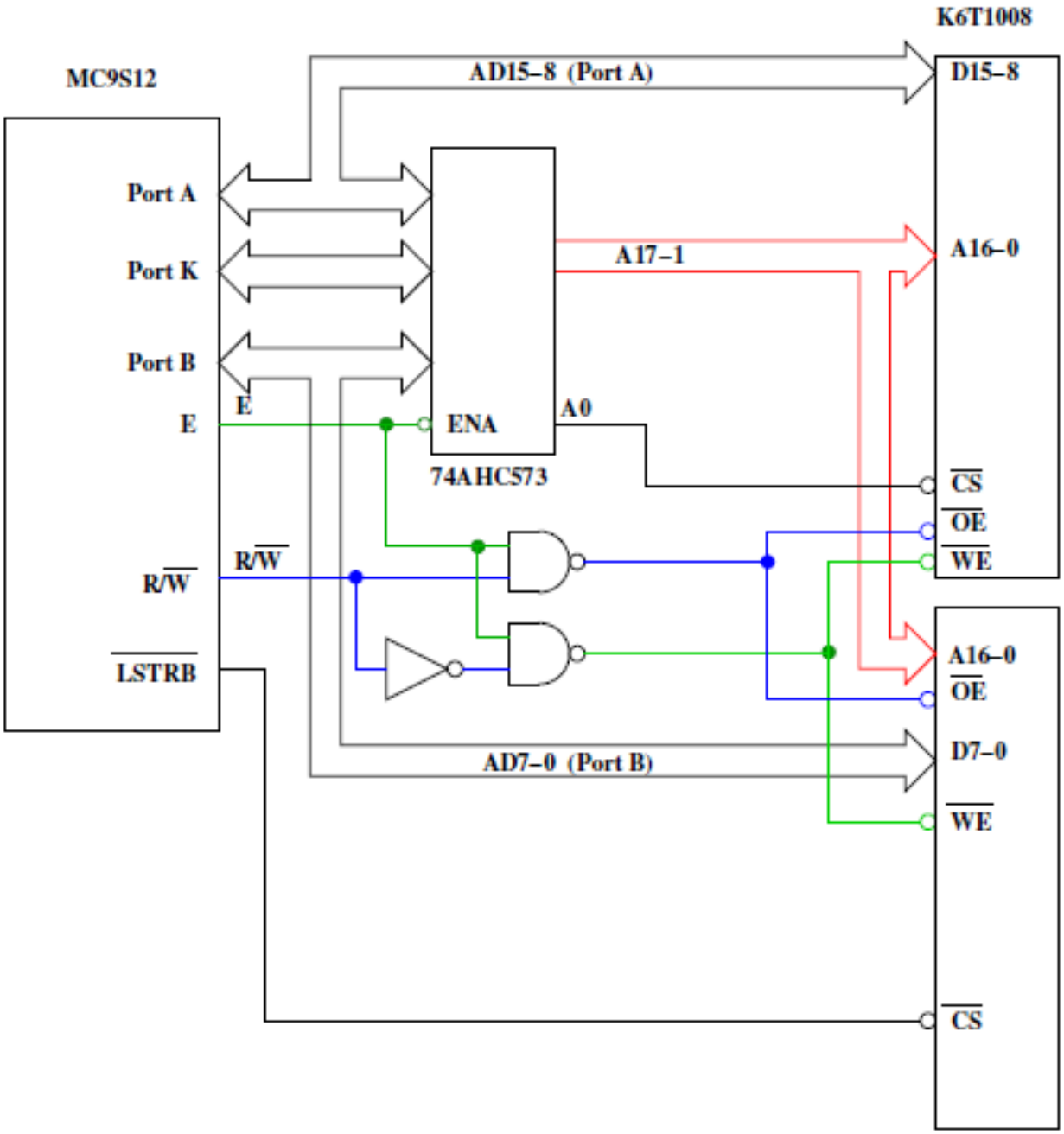
– The **CALL** instruction pushes the 16-bit return address and the current 8-bit page register (PPAGE) onto the stack and then transfers control to the subroutine (3 bytes are pushed onto the stack).
CALL **<opr>** is a instruction designed to work with expanded memory. The MC9S12 treat the 16-kB memory space from $8000 to $BFFF as a program memory window. The **<opr>** field in the call instruction specifies the page number and the starting address of the subroutine within that page. The new page number is loaded into PPAGE when the call instruction is executed.

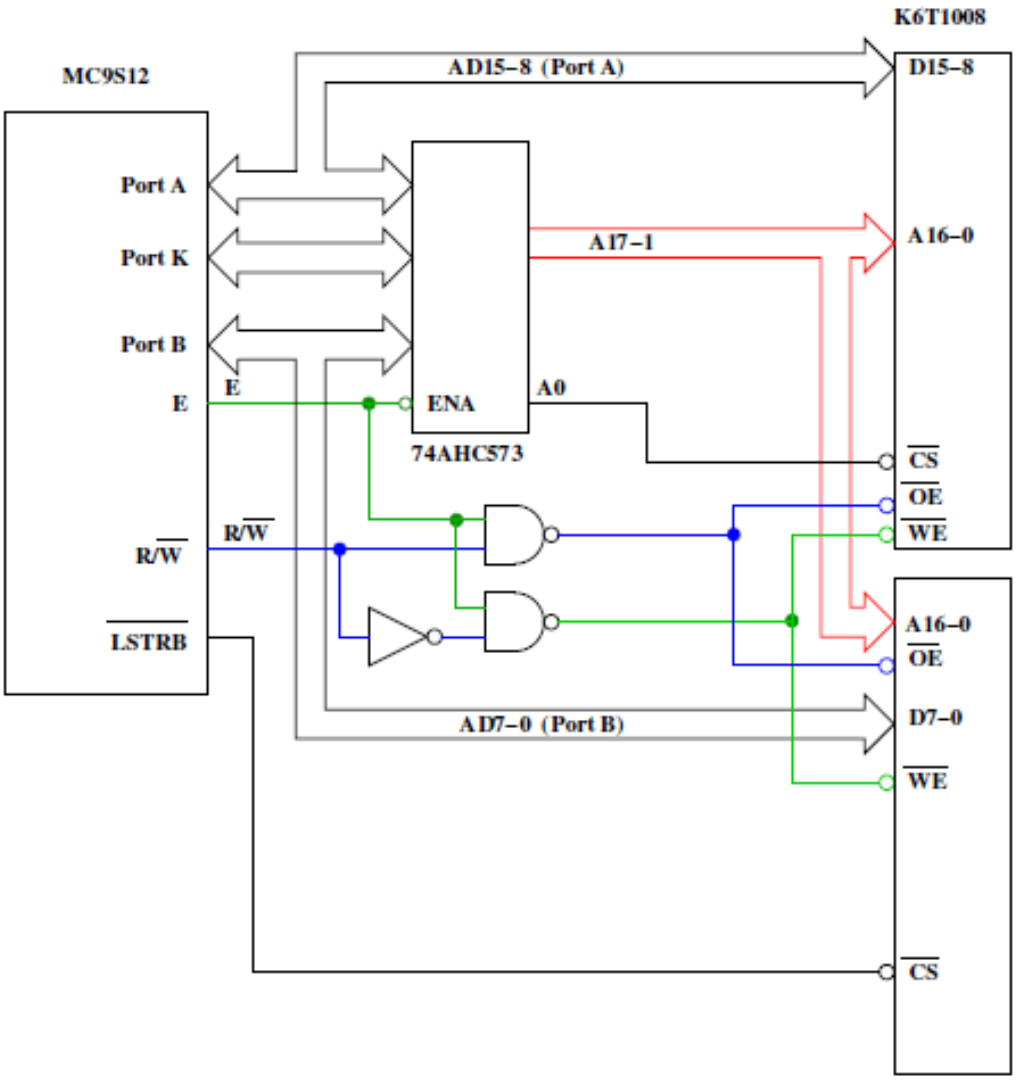
– The **RTC** (Return from Call) terminates subroutines in expanded mode invoked by the CALL instruction and pulls the return address and page register from the stack.

- The Samsung K6T1008C2E RAM require the following signals:

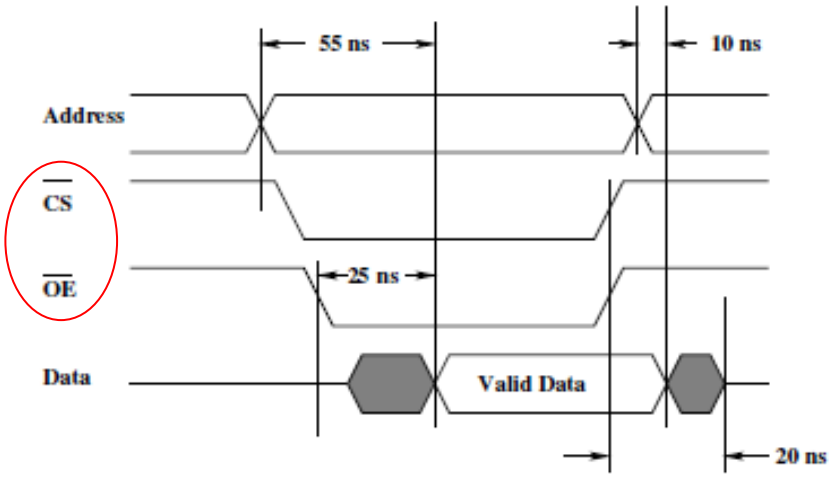
Name	Function
$\overline{CS_1}$, CS_2	Chip Select Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O_1~I/O_8	Data Inputs/Outputs
A_0~A_{16}	Address Inputs
Vcc	Power
Vss	Ground
N.C.	No Connection

Schematic of Memory Expansion





READ CYCLE (Samsung KST108C2E)



Bus clock frequency needed for memory expansion

• The control signals for the memory are generated by the MC9S12 and the glue logic.

• With a 24 MHz bus clock, the time E-clock is high is about 21 ns.

• The memory chip needs the address stable for 55 ns before it can get the data out of its memory.

• The memory cannot work with an MC9S12 using a 24 MHz clock.

• With an 8 MHz oscillator, the MC9S12 can use a bus clock of 8 MHz, 16 MHz or 24 MHz.

• To have the address stable for 55 ns, the clock period must be greater than 110 ns, which corresponds to a 9 MHz frequency.

• To have the address stable for 55 ns, the bus clock frequency must be less than 9 MHz. The expansion board uses an 8 MHz bus clock.

• With an 8 MHz clock, the clock period is 125 ns. E is high for about 62 ns, and low for about 62 ns.

• **Assume 3 ns for signals to propagate through the glue logic chips**.

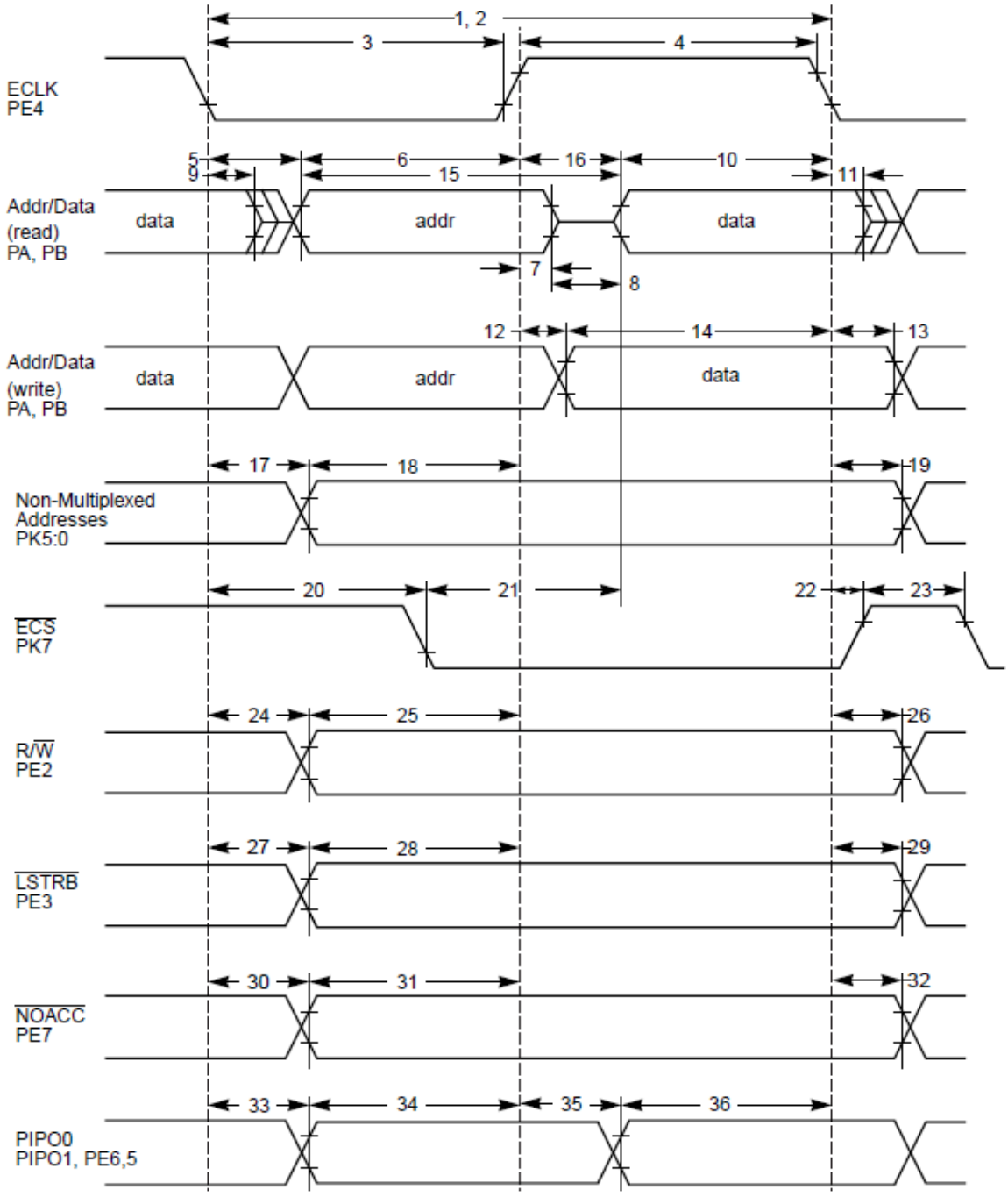


Figure A-9 General External Bus Timing

Table A-20 Expanded Bus Timing Characteristics

Conditions are shown in **Table A-4** unless otherwise noted, C_{LOAD} = 50pF							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Frequency of operation (E-clock)	f_o	0		25.0	MHz
2	P	Cycle time	t_{cyc}	40			ns
3	D	Pulse width, E low	PW_{EL}	19			ns
4	D	Pulse width, E high[1]	PW_{EH}	19			ns
5	D	Address delay time	t_{AD}			8	ns
6	D	Address valid time to E rise (PW_{EL}–t_{AD})	t_{AV}	11			ns
7	D	Muxed address hold time	t_{MAH}	2			ns
8	D	Address hold to data valid	t_{AHDS}	7			ns
9	D	Data hold to address	t_{DHA}	2			ns
10	D	Read data setup time	t_{DSR}	13			ns
11	D	Read data hold time	t_{DHR}	0			ns
12	D	Write data delay time	t_{DDW}			7	ns
13	D	Write data hold time	t_{DHW}	2			ns
14	D	Write data setup time(1) (PW_{EH}–t_{DDW})	t_{DSW}	12			ns
15	D	Address access time(1) (t_{cyc}–t_{AD}–t_{DSR})	t_{ACCA}	19			ns
16	D	E high access time(1) (PW_{EH}–t_{DSR})	t_{ACCE}	6			ns
17	D	Non-multiplexed address delay time	t_{NAD}			6	ns
18	D	Non-muxed address valid to E rise (PW_{EL}–t_{NAD})	t_{NAV}	15			ns
19	D	Non-multiplexed address hold time	t_{NAH}	2			ns
20	D	Chip select delay time	t_{CSD}			16	ns
21	D	Chip select access time(1) (t_{cyc}–t_{CSD}–t_{DSR})	t_{ACCS}	11			ns
22	D	Chip select hold time	t_{CSH}	2			ns
23	D	Chip select negated time	t_{CSN}	8			ns
24	D	Read/write delay time	t_{RWD}			7	ns
25	D	Read/write valid time to E rise (PW_{EL}–t_{RWD})	t_{RWV}	14			ns
26	D	Read/write hold time	t_{RWH}	2			ns
27	D	Low strobe delay time	t_{LSD}			7	ns
28	D	Low strobe valid time to E rise (PW_{EL}–t_{LSD})	t_{LSV}	14			ns
29	D	Low strobe hold time	t_{LSH}	2			ns
30	D	NOACC strobe delay time	t_{NOD}			7	ns
31	D	NOACC valid time to E rise (PW_{EL}–t_{NOD})	t_{NOV}	14			ns

Memory Read

- CS for even memory chip
    1. E goes low
    2. 8 ns later, AD15-0 change into address (**MC9S12 spec**)
    3. 3 ns later, A15-0 comes out of 74AHC573 (**glue logic**)
    4. CS goes low 11 ns after E goes low. (**Total**)

- CS for odd chip is $\overline{\text{LSTRB}}$; CS for odd chip goes low 7 ns after E goes low

- Output Enable (OE)
    1. E goes high
    2. 3 ns later, OE goes low (**glue logic**)
    3. OE goes low 3 ns after E goes high (**Total**)

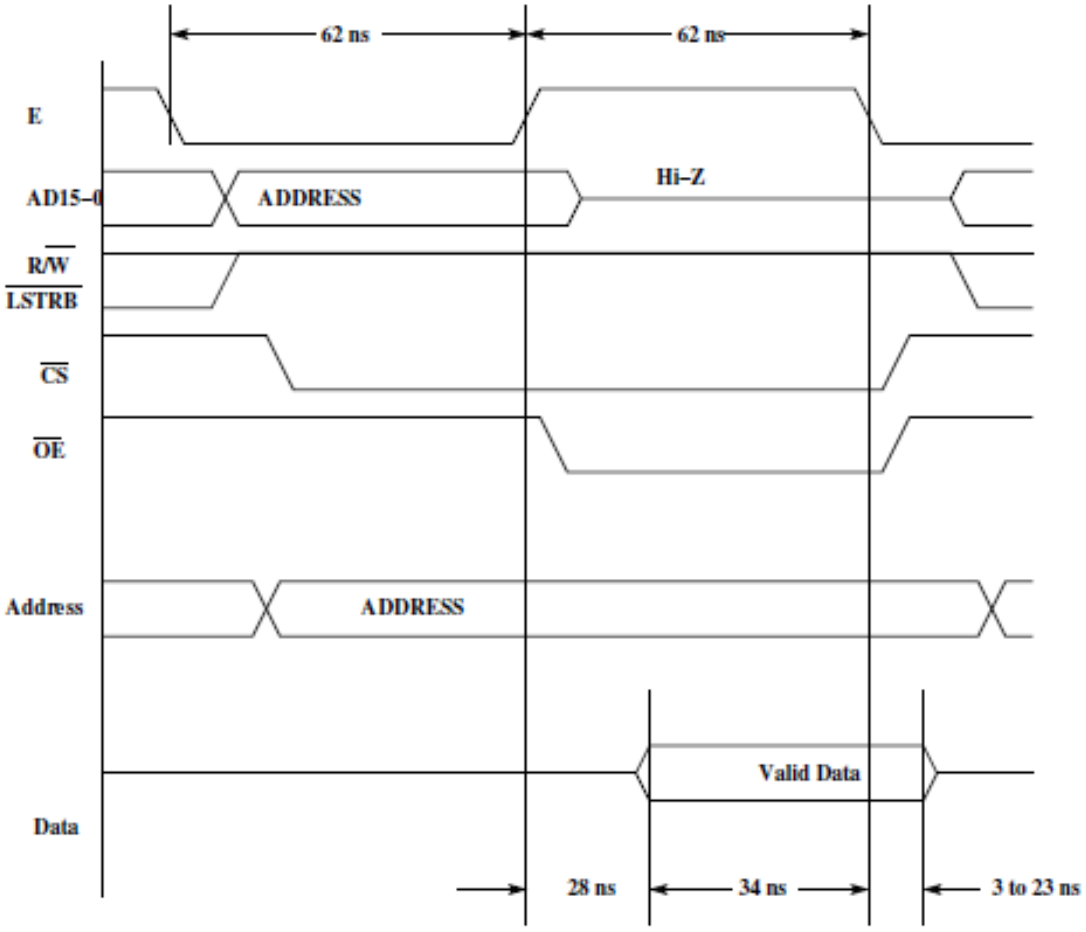
- Valid Data from Memory
    1. E goes low
    2. 8 ns later, AD15-0 change into address (**MC9S12**)
    3. 3 ns later, A15-0 comes out of 74AHC573 (**glue logic**)
    4. 55 ns later, valid data is available from memory chip (**memory**)
    5. 66 ns after E goes low, valid data is available (**but not on bus**) (**Total**)

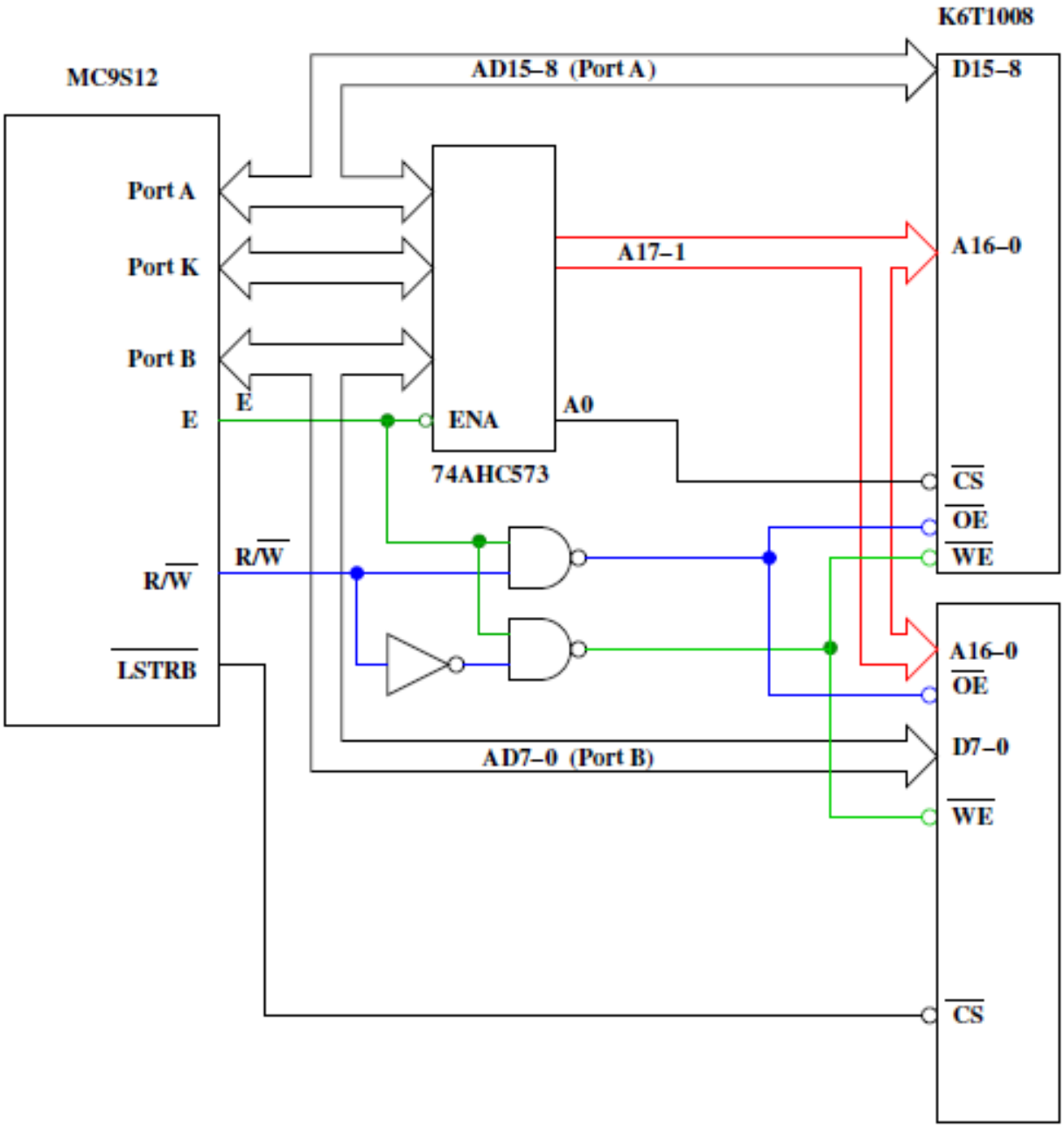
- Data from Memory put onto bus
    1. E goes high
    2. 3 ns later, OE goes low (**glue logic**)
    3. 25 ns later, memory chip puts data onto bus (**memory**)
    4. 28 ns after E goes high, data from memory is put onto bus (**total**)

- MC9S12 reads data
    1. MC9S12 needs data on bus 13 ns before E goes low (**MC9S12**)
    2. E goes low 62 ns - 28 ns = 34 ns before E goes low (**Total**)
    3. This meets the MC9S12 data setup time

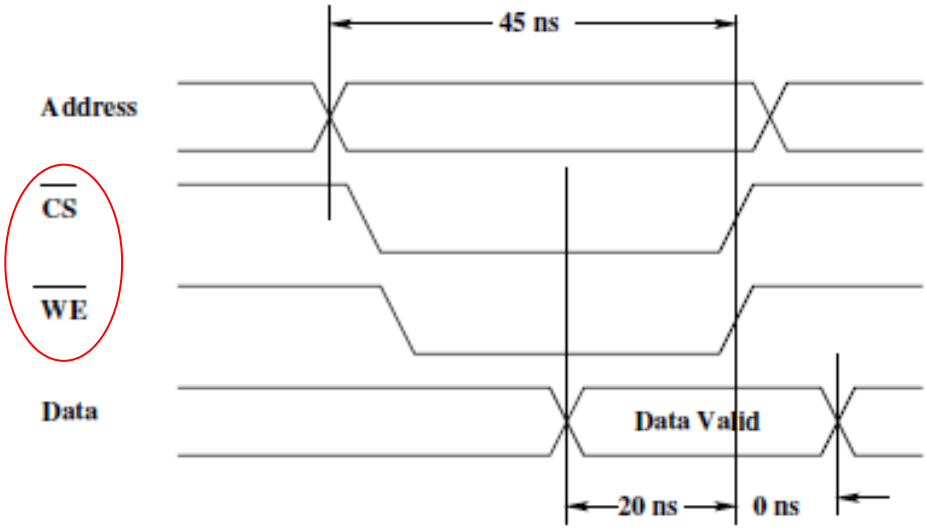
- Data removed from bus
    1. MC9S12 needs data on bus 0 ns after E goes low (**MC9S12**)
    2. OE goes high 3 ns after E goes low (**glue logic**)
    3. Data removed from bus 0 to 20 ns after OE goes high (**memory**)
    4. Data on bus 3 ns to 23 ns after E goes low (**Total**)
    5. This meets the MC9S12 data hold time

- The memory chip will work with the RAM for read cycles when the MC9S12 uses an 8 MHz bus clock


62 ns
62 ns
E
AD15–0
ADDRESS
Hi–Z
R/W
LSTRB
CS
OE
Address
ADDRESS
Valid Data
Data
28 ns
34 ns
3 to 23 ns


K6T1008
MC9S12
AD15–8 (Port A)
D15–8
Port A
Port K
Port B
A17–1
A16–0
E
E
ENA
A0
74AHC573
CS
OE
WE
R/W
R/W
LSTRB
A16–0
OE
D7–0
AD7–0 (Port B)
WE
CS

WRITE CYCLE (Samsung KST1008C2E)



Memory Write

- CS for even memory chip. CS for even memory chip is A0.
    1. E goes low
    2. 8 ns later, AD15-0 change into address (**MC9S12**)
    3. 3 ns later, A15-0 comes out of 74AHC573 (**glue logic**)
    4. CS goes low 11 ns after E goes low (**Total**)

- CS for odd chip is $\overline{\text{LSTRB}}$; CS for odd chip goes low 7 ns after E goes low

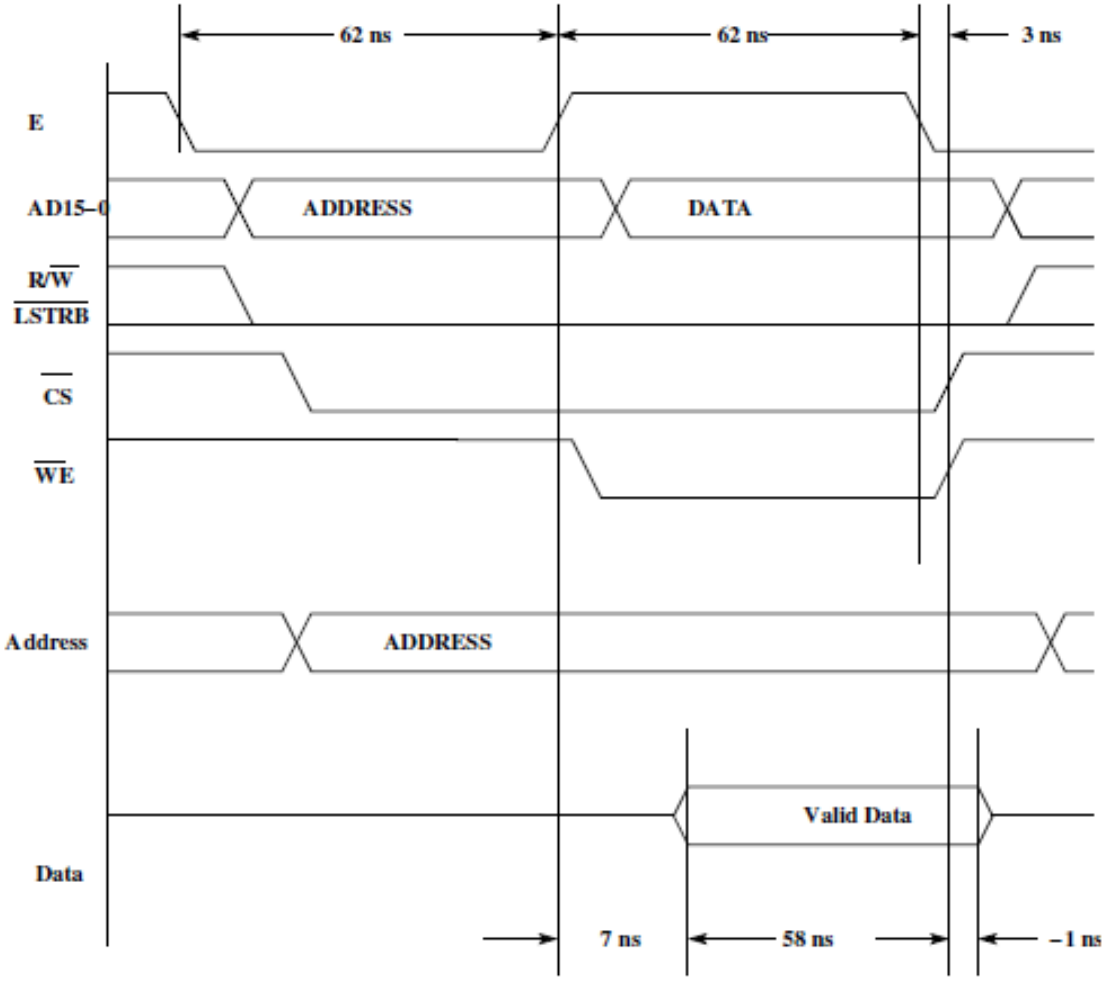
- Write Enable (WE)
    1. E goes high
    2. 3 ns later, WE goes low (**glue logic**)
    3. WE goes low 3 ns after E goes high (**Total**)

- MC9S12 puts data on bus
    1. E goes high
    2. 7 ns later, AD15-0 change into data (**MC9S12**)
    3. 7 ns after E goes high, MC9S12 puts data on bus (**MC9S12**)

- Memory latches data
    1. E goes low
    2. 3 ns later, WE goes high (**glue logic**)
    3. Memory needs data on bus 20 ns before WE goes high (**memory**)
    4. Data is on bus 58 ns before WE goes high (**Total**)
    5. This meets the memory write setup time

- Data removed from bus
    1. Memory needs data on bus 0 ns after WE goes high (**memory**)
    2. WE goes high 3 ns after E goes low (**glue logic**)
    3. Data removed from bus 2 ns after E goes low (**MC9S12**)
    4. Data on bus -1 ns WE goes high (**Total**)
    5. **Close**; will probably meet specs

- The memory chip will work with the RAM for write cycles


62 ns
62 ns
3 ns
E
AD15–0
ADDRESS
DATA
R/W
LSTRB
CS
WE
Address
ADDRESS
Valid Data
Data
7 ns
58 ns
–1 ns

A Faster Memory Chip

• Access time of a memory chip is usually the amount of time from when the chip is selected to the data being available

• For a MC9S12 with a 24 MHz clock, time from address available to time MC9S12 needs data to be ready is [6] + [4], or 11 ns + 19 ns = 30 ns. It will take a few nanoseconds for the glue logic to latch the address, and determine if the chip should be selected. For the circuit shown, there are two propagation delays between a new address available and the chip being selected, so if this is 6 ns, the access time of the memory chip must be less than 30 ns - 6 ns = 24 ns.

• A 12 ns memory chip would probably work for interfacing to the MC9S12 with a 24 MHz bus clock.