

- **MC9S12 Assembler Directives**
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  - Assembler directives
  - How to disassemble an MC9S12 instruction sequence

Summary of HCS12 addressing modes

**ADDRESSING MODES**

Name	Example	Op Code	Effective Address
<b>INH</b> <b>Inherent</b>	<b>ABA</b>	<b>18 06</b>	<b>None</b>
<b>IMM</b> <b>Immediate</b>	<b>LDAA #35</b>	<b>86 35</b>	<b>PC + 1</b>
<b>DIR</b> <b>Direct</b>	<b>LDAA \$35</b>	<b>96 35</b>	<b>0x0035</b>
<b>EXT</b> <b>Extended</b>	<b>LDAA \$2035</b>	<b>B6 20 35</b>	<b>0x2035</b>
<b>IDX</b> <b>Indexed</b>	<b>LDAA 3, X</b>	<b>A6 03</b>	<b>X + 3</b>
<b>IDX1</b>	<b>LDAA 30, X</b>	<b>A6 E0 13</b>	<b>X + 30</b>
<b>IDX2</b>	<b>LDAA 300, X</b>	<b>A6 E2 01 2C</b>	<b>X + 300</b>
<b>IDX</b> <b>Indexed Postincrement</b>	<b>LDAA 3, X+</b>	<b>A6 32</b>	<b>X (X+3 -&gt; X)</b>
<b>IDX</b> <b>Indexed Preincrement</b>	<b>LDAA 3, +X</b>	<b>A6 22 </b>	<b>X+3 (X+3 -&gt; X)</b>
<b>IDX</b> <b>Indexed Postdecrement</b>	<b>LDAA 3, X-</b>	<b>A6 3D</b>	<b>X (X-3 -&gt; X)</b>
<b>IDX</b> <b>Indexed Predecrement</b>	<b>LDAA 3, -X</b>	<b>A6 2D</b>	<b>X-3 (X-3 -&gt; X)</b>
<b>REL</b> <b>Relative</b>	<b>BRA \$1050</b> <b>LBRA \$1F00</b>	<b>20 23</b> <b>18 20 0E CF</b>	<b>PC + 2 + Offset</b> <b>PC + 4 + Offset</b>

**A few instructions have two effective addresses:**

- **MOVB # $\$AA$ , $\$1C00$**  Move byte 0xAA (IMM) to address \$1C00 (EXT)
- **MOVW 0,X,0,Y** Move word from address pointed to by X (IDX) to address pointed to by Y (IDX)

**A few instructions have three effective addresses:**

- **BRSET FOO,# $\$03$ ,LABEL** Branch to LABEL (REL) if bits # $\$03$  (IMM) of variable FOO (EXT) are set.

## Using X and Y as Pointers

- Registers X and Y are often used to point to data.
- To initialize pointer use

**ldx #table**

not

**ldx table**

- For example, the following loads the address of table (\$1000) into X; i.e., X will point to table:

**ldx #table ; *Address of table* ⇒ X**

The following puts the first two bytes of table (\$0C7A) into X. X will **not** point to table:

**ldx table ; *First two bytes of table* ⇒ X**

- To step through table, need to increment pointer after use

**ldaa 0,x**

**inx**

or

**ldaa 1,x+**

```
table
```

0C
7A
D5
00
61
62
63
64

```
table:  org    $900
        dc.b  12,122,-43,0
        dc.b  'a','b','c','d'
```

### Which branch instruction should you use?

Branch if A > B

Is 0xFF > 0x00?

If unsigned, 0xFF = 255 and 0x00 = 0,  
so 0xFF > 0x00

If signed, 0xFF = -1 and 0x00 = 0,  
so 0xFF < 0x00

Using unsigned numbers: **BHI** (checks C bit of CCR)

Using signed numbers: **BGT** (checks V bit of CCR)

For unsigned numbers, use branch instructions which check C bit

For signed numbers, use branch instructions which check V bit

## **Hand Assembling a Program**

To hand-assemble a program, do the following:

1. Start with the **org** statement, which shows where the first byte of the program will go into memory.

(e.g., **org \$2000** will put the first instruction at address **\$2000**.)

2. Look at the first instruction. Determine the addressing mode used.

(e.g., **ldab #10** uses IMM mode.)

3. Look up the instruction in the **MC9S12 S12CPUV2 Reference Manual**, find the appropriate Addressing Mode, and the Object Code for that addressing mode. (e.g., **ldab IMM** has object code **C6 ii**.)

- **Table A.1 of the S12CPUV2 Reference Manual** has a concise summary of the instructions, addressing modes, op-codes, and cycles.

4. Put in the object code for the instruction, and put in the appropriate operand. Be careful to convert decimal operands to hex operands if necessary. (e.g., **ldab #10** becomes **C6 0A**.)

5. Add the number of bytes of this instruction to the address of the instruction to determine the address of the next instruction.

(e.g., **\$2000 + 2 = \$2002** will be the starting address of the next instruction.)

```
org $2000
ldab #10
loop: clra
      dbne b,loop
      swi
```

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Abs.	Rel.	Loc	Obj. code	Source line
1	1			
2	2	0000	2000	prog: equ \$2000
3	3			org prog
4	4	a002000	C60A	ldab #10
5	5	a002002	87	loop: clra
6	6	a002003	0431 FC	dbne b,loop
7	7	a002006	3F	swi

**Table A-1. Instruction Set Summary (Sheet 7 of 14)**

Source Form	Operation	Addr. Mode	Machine Coding (hex)	Access Detail		S X H I	N Z V C
				HCS12	M68HC12		
LBGT <i>rel</i> <i>s</i>	Long Branch if Greater Than (if $Z + (N \oplus V) = 0$ ) (signed)	REL	18 2E qq rr	OPPP/OPO <sup>1</sup>	OPPP/OPO <sup>1</sup>	----	----
LBHI <i>rel</i> <i>ts</i>	Long Branch if Higher (if $C + Z = 0$ ) (unsigned)	REL	18 22 qq rr	OPPP/OPO <sup>1</sup>	OPPP/OPO <sup>1</sup>	----	----
LBHS <i>rel</i> <i>s</i>	Long Branch if Higher or Same (if $C = 0$ ) (unsigned) same function as LBCC	REL	18 24 qq rr	OPPP/OPO <sup>1</sup>	OPPP/OPO <sup>1</sup>	----	----
LBLT <i>rel</i> <i>s</i>	Long Branch if Less Than or Equal (if $Z + (N \oplus V) = 1$ ) (signed)	REL	18 2F qq rr	OPPP/OPO <sup>1</sup>	OPPP/OPO <sup>1</sup>	----	----
LBLO <i>rel</i> <i>ts</i>	Long Branch if Lower (if $C = 1$ ) (unsigned) same function as LBCCS	REL	18 25 qq rr	OPPP/OPO <sup>1</sup>	OPPP/OPO <sup>1</sup>	----	----
LBLS <i>rel</i> <i>s</i>	Long Branch if Lower or Same (if $C + Z = 1$ ) (unsigned)	REL	18 23 qq rr	OPPP/OPO <sup>1</sup>	OPPP/OPO <sup>1</sup>	----	----
LBMT <i>rel</i> <i>ts</i>	Long Branch if Minus (if $N = 1$ )	REL	18 2B qq rr	OPPP/OPO <sup>1</sup>	OPPP/OPO <sup>1</sup>	----	----
LBNE <i>rel</i> <i>s</i>	Long Branch if Not Equal (if $Z = 0$ )	REL	18 26 qq rr	OPPP/OPO <sup>1</sup>	OPPP/OPO <sup>1</sup>	----	----
LBPL <i>rel</i> <i>s</i>	Long Branch if Plus (if $N = 0$ )	REL	18 2A qq rr	OPPP/OPO <sup>1</sup>	OPPP/OPO <sup>1</sup>	----	----
LBRA <i>rel</i> <i>s</i>	Long Branch Always (if 1=1)	REL	18 20 qq rr	OPPP	OPPP	----	----
LBRA <i>rel</i> <i>ts</i>	Long Branch Always (if 1=1)	REL	18 20 qq rr	OPPP	OPPP	----	----
LBRN <i>rel</i> <i>ts</i>	Long Branch Never (if 1=0)	REL	18 21 qq rr	OPO	OPO	----	----
LBVC <i>rel</i> <i>s</i>	Long Branch if Overflow Bit Clear (if $V=0$ )	REL	18 28 qq rr	OPPP/OPO <sup>1</sup>	OPPP/OPO <sup>1</sup>	----	----
LBVS <i>rel</i> <i>ts</i>	Long Branch if Overflow Bit Set (if $V=1$ )	REL	18 29 qq rr	OPPP/OPO <sup>1</sup>	OPPP/OPO <sup>1</sup>	----	----
LDA <i>#opr</i> <i>s</i> LDA <i>opr</i> <i>s</i> LDA <i>opr</i> <i>ts</i> LDA <i>opr</i> <i>ts</i> <i>xy</i> <i>sp</i> LDA <i>opr</i> <i>ts</i> <i>xy</i> <i>sp</i> LDA <i>opr</i> <i>ts</i> <i>xy</i> <i>sp</i> LDA <i>[D,xy]</i> <i>sp</i> LDA <i>[opr,ts,xy]</i>	(M) → A Load Accumulator A	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	86 11 96 dd B6 bh 11 A6 xb A6 xb ff A6 xb aa ff A6 xb A6 xb aa ff	P zPE zPO zPE zPO EzPP EzPEzPE EzPEzPE	P zFP zOP zFP zPO EzPP EzFPzFP EzPEzFP	----	AAA-
LDB <i>#opr</i> <i>s</i> LDB <i>opr</i> <i>s</i> LDB <i>opr</i> <i>ts</i> LDB <i>opr</i> <i>ts</i> <i>xy</i> <i>sp</i> LDB <i>opr</i> <i>ts</i> <i>xy</i> <i>sp</i> LDB <i>opr</i> <i>ts</i> <i>xy</i> <i>sp</i> LDB <i>[D,xy]</i> <i>sp</i> LDB <i>[opr,ts,xy]</i>	(M) → B Load Accumulator B	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	C6 11 D6 dd F6 bh 11 B6 xb B6 xb ff B6 xb aa ff B6 xb B6 xb aa ff	P zPE zPO zPE zPO EzPP EzPEzPE EzPEzPE	P zFP zOP zFP zPO EzPP EzFPzFP EzPEzFP	----	AAA-
LDD <i>#opr</i> <i>ts</i> LDD <i>opr</i> <i>ts</i> LDD <i>opr</i> <i>ts</i> LDD <i>opr</i> <i>ts</i> <i>xy</i> <i>sp</i> LDD <i>opr</i> <i>ts</i> <i>xy</i> <i>sp</i> LDD <i>opr</i> <i>ts</i> <i>xy</i> <i>sp</i> LDD <i>[D,xy]</i> <i>sp</i> LDD <i>[opr,ts,xy]</i>	(M+1) → A:B Load Double Accumulator D (A:B)	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	CC j j kk DC dd FC bh 11 BC xb BC xb ff BC xb aa ff BC xb BC xb aa ff	PO zPE zPO zPE zPO EzPP EzPEzPE EzPEzPE	OP zFP zOP zFP zPO EzPP EzFPzFP EzPEzFP	----	AAA-

Note 1. OPPP/OPO indicates this instruction takes four cycles to refill the instruction queue if the branch is taken and three cycles if the branch is not taken.

**Table A-1. Instruction Set Summary (Sheet 3 of 14)**

Source Form	Operation	Addr. Mode	Machine Coding (hex)	HCS12	Access Detail M68HC12	S X H I	N Z V C
BLS <i>nb</i>	Branch if Lower or Same (if C + Z = 1) (unsigned)	REL	23 <i>rr</i>	<i>ppp/p<sup>1</sup></i>	<i>ppp/p<sup>1</sup></i>	----	----
BLT <i>nb</i>	Branch if Less Than (if N ⊕ V = 1) (signed)	REL	2D <i>rr</i>	<i>ppp/p<sup>1</sup></i>	<i>ppp/p<sup>1</sup></i>	----	----
BMI <i>nb</i>	Branch if Minus (if N = 1)	REL	2B <i>rr</i>	<i>ppp/p<sup>1</sup></i>	<i>ppp/p<sup>1</sup></i>	----	----
BNE <i>nb</i>	Branch if Not Equal (if Z = 0)	REL	26 <i>rr</i>	<i>ppp/p<sup>1</sup></i>	<i>ppp/p<sup>1</sup></i>	----	----
BPL <i>nb</i>	Branch if Plus (if N = 0)	REL	2A <i>rr</i>	<i>ppp/p<sup>1</sup></i>	<i>ppp/p<sup>1</sup></i>	----	----
BRA <i>nb</i>	Branch Always (if 1 = 1)	REL	20 <i>rr</i>	<i>ppp</i>	<i>ppp</i>	----	----
BRCLR <i>opn16, mask, nb</i> BRCLR <i>opn16, mask, nb</i> BRCLR <i>opn02_xy, mask, nb</i> BRCLR <i>opn02_xy, mask, nb</i> BRCLR <i>opn16_xy, mask, nb</i>	Branch if (M) ⊕ (imm) = 0 (if All Selected Bit(s) Clear)	DIR EXT IDX IDX1 IDX2	4F <i>dd mm rr</i> 1F <i>hh ll mm rr</i> 0F <i>xb mm rr</i> 0F <i>xb ff mm rr</i> 0F <i>xb oo ff mm rr</i>	<i>ppp</i> <i>ppppp</i> <i>ppp</i> <i>ppppp</i> <i>pppppp</i>	<i>ppp</i> <i>ppppp</i> <i>ppp</i> <i>ppppp</i> <i>pppppp</i>	----	----
BRN <i>nb</i>	Branch Never (if 1 = 0)	REL	21 <i>rr</i>	<i>p</i>	<i>p</i>	----	----
BRSET <i>opn16, mask, nb</i> BRSET <i>opn16, mask, nb</i> BRSET <i>opn02_xy, mask, nb</i> BRSET <i>opn02_xy, mask, nb</i> BRSET <i>opn16_xy, mask, nb</i>	Branch if (M) ⊕ (imm) = 0 (if All Selected Bit(s) Set)	DIR EXT IDX IDX1 IDX2	4E <i>dd mm rr</i> 1E <i>hh ll mm rr</i> 0E <i>xb mm rr</i> 0E <i>xb ff mm rr</i> 0E <i>xb oo ff mm rr</i>	<i>ppp</i> <i>ppppp</i> <i>ppp</i> <i>ppppp</i> <i>pppppp</i>	<i>ppp</i> <i>ppppp</i> <i>ppp</i> <i>ppppp</i> <i>pppppp</i>	----	----
BSET <i>opn16, mask</i> BSET <i>opn16, mask</i> BSET <i>opn02_xy, mask</i> BSET <i>opn02_xy, mask</i> BSET <i>opn16_xy, mask</i>	(M) ⊕ (imm) → M Set Bit(s) in Memory	DIR EXT IDX IDX1 IDX2	4C <i>dd mm</i> 1C <i>hh ll mm</i> 0C <i>xb mm</i> 0C <i>xb ff mm</i> 0C <i>xb oo ff mm</i>	<i>ppw</i> <i>ppw</i> <i>ppw</i> <i>ppw</i> <i>ppppp</i>	<i>ppw</i> <i>ppw</i> <i>ppw</i> <i>ppw</i> <i>ppppp</i>	----	A A 0 -
BSR <i>nb</i>	(SP) - 2 → SP; RTN <sub>C</sub> RTN <sub>L</sub> → M <sub>(SP)</sub> M <sub>(SP+1)</sub> Subroutine address → PC Branch to Subroutine	REL	07 <i>rr</i>	<i>pppp</i>	<i>pppp</i>	----	----
BVC <i>nb</i>	Branch if Overflow Bit Clear (if V = 0)	REL	28 <i>rr</i>	<i>ppp/p<sup>1</sup></i>	<i>ppp/p<sup>1</sup></i>	----	----
BVS <i>nb</i>	Branch if Overflow Bit Set (if V = 1)	REL	29 <i>rr</i>	<i>ppp/p<sup>1</sup></i>	<i>ppp/p<sup>1</sup></i>	----	----
CALL <i>opn16, page</i> CALL <i>opn02_xy, page</i> CALL <i>opn02_xy, page</i> CALL <i>opn16_xy, page</i> CALL <i>[D_xy]</i> CALL <i>[opn16_xy]</i>	(SP) - 2 → SP; RTN <sub>C</sub> RTN <sub>L</sub> → M <sub>(SP)</sub> M <sub>(SP+1)</sub> (SP) - 1 → SP; PPG → M <sub>(SP)</sub> pg → PPAGE register; Program address → PC  Call subroutine in extended memory (Program may be located on another expansion memory page.)  Indirect modes get program address and new pg value based on pointer.	EXT IDX IDX1 IDX2 (D,IDX) (IDX2)	4A <i>hh ll pg</i> 4B <i>xb pg</i> 4B <i>xb ff pg</i> 4B <i>xb oo ff pg</i> 4B <i>xb</i> 4B <i>xb oo ff</i>	<i>gnpppp</i> <i>gnpppp</i> <i>gnpppp</i> <i>gnpppp</i> <i>gnpppp</i> <i>gnpppp</i>	<i>gnpppp</i> <i>gnpppp</i> <i>gnpppp</i> <i>gnpppp</i> <i>gnpppp</i> <i>gnpppp</i>	----	----
CBA	(A) - (B) Compare 8-Bit Accumulators	INH	18 17	00	00	----	A A A A
CLC	0 → C Translate b ANDCC # <i>FE</i>	IMM	10 FE	<i>p</i>	<i>p</i>	----	---0
CLI	0 → I Translate b ANDCC # <i>EF</i> (enables I-bit interrupts)	IMM	10 EF	<i>p</i>	<i>p</i>	----	---0
CLR <i>opn16</i> CLR <i>opn02_xy</i> CLR <i>opn02_xy</i> CLR <i>opn16_xy</i> CLR <i>[D_xy]</i> CLR <i>[opn16_xy]</i> CLRA CLRB	0 → M Clear Memory Location  0 → A Clear Accumulator A 0 → B Clear Accumulator B	EXT IDX IDX1 IDX2 (D,IDX) (IDX2) INH INH	79 <i>hh ll</i> 69 <i>xb</i> 69 <i>xb ff</i> 69 <i>xb oo ff</i> 69 <i>xb</i> 69 <i>xb oo ff</i> 87 C7	<i>ppw</i> <i>ppw</i> <i>ppw</i> <i>ppw</i> <i>pppw</i> <i>pppw</i> 0 0	<i>wpp</i> <i>ppw</i> <i>ppw</i> <i>ppw</i> <i>pppw</i> <i>pppw</i> 0 0	----	0 1 0 0
CLV	0 → V Translate b ANDCC # <i>FD</i>	IMM	10 FD	<i>p</i>	<i>p</i>	----	---0-

Note 1. PPPP indicates this instruction takes three cycles to refill the instruction queue if the branch is taken and one program latch cycle if the branch is not taken.



**Table A-1. Instruction Set Summary (Sheet 4 of 14)**

Source Form	Operation	Addr. Mode	Machine Coding (hex)	Access Detail		SXHI	NZVC
				HCS12	M68HC12		
CMPB #opr16 CMPB opr16 CMPB opr16a CMPB opr16_xyop CMPB opr16_xyasp CMPB [D_xyasp] CMPB [opr16_xyasp]	(B) - (M) Compare Accumulator B with Memory	IMM DIR EXT IDX IDX1 IDX2 (D,IDX) (IDX2)	C1 11 D1 dd F1 hh 11 E1 xb E1 xb ff E1 xb oo ff E1 xb oo ff	F zPF zPO zPF zPO zPF zPFzPF zPFzPF	F zPF zPO zPF zPO zPF zPFzPF zPFzPF	----	AAAA
COM #opr16a COM opr16_xyop COM opr16_xyasp COM opr16_xyasp COM [D_xyasp] COM [opr16_xyasp] COMA COMB	(M) → M equivalent to \$FF - (M) → M 1's Complement Memory Location  (A) → A Complement Accumulator A (B) → B Complement Accumulator B	EXT IDX IDX1 IDX2 (D,IDX) (IDX2) INH INH	71 hh 11 61 xb 61 xb ff 61 xb oo ff 61 xb 61 xb oo ff 41 51	zPW zPW zPW zPW zPFzPW zPFzPW O O	zPW zPW zPW zPW zPFzPW zPFzPW O O	----	AA01
CPD #opr16 CPD opr16 CPD opr16a CPD opr16_xyop CPD opr16_xyasp CPD opr16_xyasp CPD [D_xyasp] CPD [opr16_xyasp]	(A,B) - (MM+1) Compare D to Memory (16-Bit)	IMM DIR EXT IDX IDX1 IDX2 (D,IDX) (IDX2)	BC jj kk 9C dd BC hh 11 AC xb AC xb ff AC xb oo ff AC xb oo ff	PO zPF zPO zPF zPO zPF zPFzPF zPFzPF	OP zPF zPO zPF zPO zPF zPFzPF zPFzPF	----	AAAA
CPS #opr16 CPS opr16 CPS opr16a CPS opr16_xyop CPS opr16_xyasp CPS opr16_xyasp CPS [D_xyasp] CPS [opr16_xyasp]	(SP) - (MM+1) Compare SP to Memory (16-Bit)	IMM DIR EXT IDX IDX1 IDX2 (D,IDX) (IDX2)	BF jj kk 9F dd BF hh 11 AF xb AF xb ff AF xb oo ff AF xb oo ff	PO zPF zPO zPF zPO zPF zPFzPF zPFzPF	OP zPF zPO zPF zPO zPF zPFzPF zPFzPF	----	AAAA
CPX #opr16 CPX opr16 CPX opr16a CPX opr16_xyop CPX opr16_xyasp CPX opr16_xyasp CPX [D_xyasp] CPX [opr16_xyasp]	(X) - (MM+1) Compare X to Memory (16-Bit)	IMM DIR EXT IDX IDX1 IDX2 (D,IDX) (IDX2)	BE jj kk 9E dd BE hh 11 AE xb AE xb ff AE xb oo ff AE xb oo ff	PO zPF zPO zPF zPO zPF zPFzPF zPFzPF	OP zPF zPO zPF zPO zPF zPFzPF zPFzPF	----	AAAA
CPY #opr16 CPY opr16 CPY opr16a CPY opr16_xyop CPY opr16_xyasp CPY opr16_xyasp CPY [D_xyasp] CPY [opr16_xyasp]	(Y) - (MM+1) Compare Y to Memory (16-Bit)	IMM DIR EXT IDX IDX1 IDX2 (D,IDX) (IDX2)	BD jj kk 9D dd BD hh 11 AD xb AD xb ff AD xb oo ff AD xb oo ff	PO zPF zPO zPF zPO zPF zPFzPF zPFzPF	OP zPF zPO zPF zPO zPF zPFzPF zPFzPF	----	AAAA
DAA	Adjust Sum to BCD Decimal Adjust Accumulator A	INH	18 07	OFO	OFO	----	AA?A
DBEQ abdxy, rel9	(cont) - 1 → cont if (cont) = 0, then Branch else Continue to next instruction  Decrement Counter and Branch if = 0 (cont = A, B, D, X, Y, or SP)	REL (9-bit)	04 1b rr	FFF (branch) FFO (no branch)	FFF	----	----
DBNE abdxy, rel9	(cont) - 1 → cont if (cont) not = 0, then Branch, else Continue to next instruction  Decrement Counter and Branch if ≠ 0 (cont = A, B, D, X, Y, or SP)	REL (9-bit)	04 1b rr	FFF (branch) FFO (no branch)	FFF	----	----

# DBNE      Decrement and Branch if Not Equal to Zero      DBNE

**Operation**     $(\text{counter}) - 1 \Rightarrow \text{counter}$   
                   If  $(\text{counter}) \text{ not } = 0$ , then  $(\text{PC}) + \$0003 + \text{rel} \Rightarrow \text{PC}$

Subtracts one from the counter register A, B, D, X, Y, or SP. Branches to a relative destination if the counter register does not reach zero. Rel is a 9-bit two's complement offset for branching forward or backward in memory. Branching range is \$100 to \$0FF (-256 to +255) from the address following the last byte of object code in the instruction.

**CCR Effects**

S	X	H	I	N	Z	V	C
-	-	-	-	-	-	-	-

**Code and CPU Cycles**

Source Form	Address Mode	Machine Code (Hex)	CPU Cycles
DBNE <i>abdxy</i> sp, <i>rel</i> 9	REL (9-bit)	04 1b rr	PPP (branch) PPO (no branch)

Source Form	Postbyte <sup>1</sup>	Object Code	Counter Register	Offset
DBNE A, <i>rel</i> 9	0010 X000	04 20 rr	A	Positive
DBNE B, <i>rel</i> 9	0010 X001	04 21 rr	B	
DBNE D, <i>rel</i> 9	0010 X100	04 24 rr	D	
DBNE X, <i>rel</i> 9	0010 X101	04 25 rr	X	
DBNE Y, <i>rel</i> 9	0010 X110	04 26 rr	Y	
DBNE SP, <i>rel</i> 9	0010 X111	04 27 rr	SP	
DBNE A, <i>rel</i> 9	0011 X000	04 30 rr	A	Negative
DBNE B, <i>rel</i> 9	0011 X001	04 31 rr	B	
DBNE D, <i>rel</i> 9	0011 X100	04 34 rr	D	
DBNE X, <i>rel</i> 9	0011 X101	04 35 rr	X	
DBNE Y, <i>rel</i> 9	0011 X110	04 36 rr	Y	
DBNE SP, <i>rel</i> 9	0011 X111	04 37 rr	SP	

NOTES:  
 1. Bits 7:6:5 select DBEQ or DBNE; bit 4 is the offset sign bit; bit 3 is not used; bits 2:1:0 select the counter register.

## MC9S12 Cycles

- MC9S12 works on **48 MHz clock**
- A processor cycle takes 2 clock cycles – P clock is 24 MHz
- Each processor cycle takes **41.7 ns** (1/24  $\mu$ s) to execute
- An instruction takes from **1 to 12** processor cycles to execute
- You can determine how many cycles an instruction takes by looking up the CPU cycles for that instruction in the Reference Manual.
  - For example, **LDAB** using the **IMM** addressing mode shows one CPU cycle (of type P).
  - **LDAB** using the **EXT** addressing mode shows three CPU cycles (of type **rPO**).
  - Section 6.6 of the S12CPUV2 Reference Manual explains what the HCS12 is doing during each of the different types of CPU cycles.

	<i>Inst</i>	<i>Mode</i>	<i>Cycles</i>
2000	<b>org \$2000</b>		
2000 C6 0A	<b>ldab #10</b>	<i>LDAB (IMM)</i>	1
2002 87	<b>loop:clra</b>	<i>CLRA (INH)</i>	1
2003 04 31 FC	<b>dbne b,loop</b>	<i>DBNE (REL)</i>	3
2006 3F	<b>swi</b>	<i>SWI</i>	9

The program executes the **ldab #10** instruction once. It then goes through the loop 10 times (which has two instructions, one with one cycle and one with three cycles), and finishes with the swi instruction (which takes 9 cycles).

Total number of cycles:

$$1 + 10 \times (1 + 3) + 9 = 50$$

$$50 \text{ cycles} = 50 \times 41.7 \text{ ns/cycle} = 2.08 \mu\text{s}$$

# LDAB

Load B

# LDAB

**Operation** (M) ⇒ B  
or  
imm ⇒ B

Loads B with either the value in M or an immediate value.

**CCR**

**Effects**

S	X	H	I	N	Z	V	C
-	-	-	-	Δ	Δ	0	-

N: Set if MSB of result is set; cleared otherwise

Z: Set if result is \$00; cleared otherwise

V: Cleared

**Code and  
CPU  
Cycles**

Source Form	Address Mode	Machine Code (Hex)	CPU Cycles
LDAB #opr8l	IMM	C6 ii	P
LDAB opr8a	DIR	D6 dd	rPE
LDAB opr16a	EXT	F6 hh ll	rPO
LDAB oprx0_xysppc	IDX	E6 xb	rPE
LDAB oprx8_xysppc	IDX1	E6 xb ff	rPO
LDAB oprx16_xysppc	IDX2	E6 xb ee ff	frPP
LDAB [D,xysppc]	[D,IDX]	E6 xb	fifrPE
LDAB [opr16,xysppc]	[IDX2]	E6 xb ee ff	fIfrPE

## **Assembler Directives**

- In order to write an assembly language program it is necessary to use assembler **directives**.
- These are not instructions which the HC12 executes but are directives to the assembler program about such things as where to put code and data into memory.
- CodeWarrior has a large number of assembler directives, which can be found in the CodeWarrior help section.
- We will use only a few of these directives. (Note: In the following table, [ ] means an optional argument.) Here are the ones we will need:

<b>Directive Name</b>	<b>Description</b>	<b>Example</b>
<b>equ</b>	Give a value to a symbol	<b>len: equ 100</b>
<b>org</b>	Set starting value of location counter where code or data will go	<b>org \$1000</b>
<b>dc.b</b>	Allocate and initialize storage for 8-bit variables. Place the bytes in successive memory locations	<b>var: dc.b 2,18</b> <b>name: dc.b "Jane"</b>
<b>dc.w</b>	Allocate and initialize storage for 16-bit variables. Place the bytes in successive memory locations	<b>var: dc.w \$ABCD</b>
<b>ds.b</b>	Allocate specified number of 8-bit storage places	<b>Table: ds.b 10</b>
<b>ds.w</b>	Allocate specified number of 16-bit storage spaces	<b>table: ds.w 50</b>
<b>dcb.b</b>	Fill memory with a given value: The first value is the number of bytes to fill. The second number is the value to put into memory	<b>init_data: dcb.b 100,0</b>

## Using labels in assembly programs

A **label** is defined by a name followed by a colon as the first thing on a line. When the label is referred to in the program, it has the numerical value of the location counter when the label was defined.

Here is a code fragment using labels and the assembler directives `dc` and `ds`:

```
        org    $2000
table1: dc.b   $23,$17,$f2,$a3,$56
table2: ds.b   5
var:   dc.w   $43af
```

The CodeWarrior assembler produces a listing file (`.lst`). Here is the listing file from the assembler:

```
Freescale HC12-Assembler
(c) Copyright Freescale 1987-2009
Abs. Rel.  Loc  Obj. code  Source line
-----
1         1                org    $2000
2         2 a002000 2317 F2A3  table1:  dc.b  $23,$17,$f2,$a3,$56
          002004 56
3         3 a002005                table2:  ds.b  5
4         4 a00200A 43AF          var:   dc.w  $43af
5         5
```

Note that **table1** is a name with the value of \$2000, the value of the location counter defined in the **org** directive. Five bytes of data



are defined by the **dc.b** directive, so the location counter is increased from \$2000 to \$2005.

Note that **table2** is a name with the value of \$2005. Five bytes of data are set aside for table2 by the **ds.b 5** directive. The as12 assembler initialized these five bytes of data to all zeros. **var** is a name with the value of \$200a, the first location after table2.

## HC12 Instructions

1. Data Transfer and Manipulation Instructions — instructions which move and manipulate data (S12CPUV2 Reference Manual, Sections 5.3, 5.4, and 5.5).

- Load and Store — load copy of memory contents into a register; store copy of register contents into memory.

LDAA \$2000 ; Copy contents of addr \$2000 into A  
STD 0,X ; Copy contents of D to addr X and X+1

- Transfer — copy contents of one register to another.

TBA ; Copy B to A  
TFR X,Y ; Copy X to Y

- Exchange — exchange contents of two registers.

XGDX ; Exchange contents of D and X  
EXG A,B ; Exchange contents of A and B

- Move — copy contents of one memory location to another.

MOVB \$2000,\$20A0 ; Copy byte at \$2000 to \$20A0  
MOVW 2,X+,2,Y+ ; Copy two bytes from address held  
; in X to address held in Y  
; Add 2 to X and Y

2. Arithmetic Instructions — addition, subtraction, multiplication, division (S12CPUV2 Reference Manual, Sections 5.6, 5.8 and 5.12).

ABA ; Add B to A; results in A  
SUBD \$20A1 ; Subtract contents of \$20A1 from D

INX                   ; Increment X by 1  
MUL                  ; Multiply A by B; results in D

3. Logic and Bit Instructions — perform logical operations  
(**S12CPUV2 Reference Manual**, Sections 5.9, 5.10, 5.11, 5.13  
and 5.14).

- Logic Instructions

    ANDA \$2000     ; Logical AND of A with contents of  
                          ; \$2000  
    EORB 2,X       ; Exclusive OR B with contents of  
                          ; address (X+2)

- Clear, Complement and Negate Instructions

    NEG -2,X       ; Negate (2's comp) contents of  
                          ; address (X-2)  
    CLRA           ; Clear ACC A

- Bit manipulate and test instructions — work with bits of a register or memory.

    BITA #\$08       ; Check to see if Bit 3 of A is set  
    BSET \$0002,#\$18 ; Set bits 3 and 4 of address \$0002

- Shift and rotate instructions

    LSLA           ; Logical shift left A  
    ASR \$1000     ; Arithmetic shift right value at address  
                          ; \$1000

4. Compare and test instructions — test contents of a register or memory (to see if zero, negative, etc.), or compare contents of a register to memory (to see if bigger than, etc.) (**S12CPUV2 Reference Manual**, Section 5.9).

TSTA ; (A)-0 -- set flags accordingly  
CPX #8000 ; (X) - 8000 -- set flags accordingly

5. Jump and Branch Instructions — Change flow of program (e.g., goto, if-then-else, switch-case) (**S12CPUV2 Reference Manual**, Sections 5.19, 5.20 and 5.21).

JMP L1 ; Start executing code at address label  
; L1  
BEQ L2 ; If Z bit set, go to label L2  
DBNE X,L3 ; Decrement X; if X not 0 then goto L3  
BRCLR \$1A,#80,L4 ; If bit 7 of addr \$1A clear, go to  
; label L4  
JSR sub1 ; Jump to subroutine sub1  
RTS ; Return from subroutine

6. Interrupt Instructions — Initiate or terminate an interrupt call (**S12CPUV2 Reference Manual**, Section 5.22).

- Interrupt instructions  
SWI ; Initiate software interrupt  
RTI ; Return from interrupt

7. Index Manipulation Instructions — Put address into X, Y or SP, manipulate X, Y or SP (**S12CPUV2 Reference Manual**, Section 5.23).

ABX                   ; Add (B) to (X)  
LEAX 5,Y           ; Put address (Y) + 5 into X

8. Condition Code Instructions — change bits in Condition Code Register (**S12CPUV2 Reference Manual**, Section 5.26).

ANDCC #\$f0       ; Clear N, Z, C and V bits of CCR  
SEV               ; Set V bit of CCR

9. Stacking Instructions — push data onto and pull data off of stack (**S12CPUV2 Reference Manual**, Section 5.24).

PSHA           ; Push contents of A onto stack  
PULX           ; Pull two top bytes of stack, put into X

10. Stop and Wait Instructions — put MC9S12 into low power mode (**S12CPUV2 Reference Manual**, Section 5.27).

STOP           ; Put into lowest power mode  
WAI           ; Put into low power mode until next interrupt

11. Null Instructions

NOP ; No operation  
BRN           ; Branch never

12. Instructions we won't discuss or use — BCD arithmetic, fuzzy logic, minimum and maximum, multiply-accumulate, table interpolation (**S12CPUV2 Reference Manual**, Sections 5.7, 5.16, 5.17, and 5.18).

### **Disassembly of an HC12 Program**

- It is sometimes useful to be able to convert *HC12 op codes* into *mnemonics*.

**For example, consider the hex code:**

ADDR DATA

-----  
1000 **C6 05** CE 20 00 **E6 01 18 06** 04 35 EE **3F**

- To determine the instructions, use Table A-2 of the HCS12 Core Users Guide.
  - If the first byte of the instruction is anything other than **\$18**, use Sheet 1 of Table A.2. From this table, determine the number of bytes of the instruction and the addressing mode. For example, **\$C6** is a two-byte instruction, the mnemonic is **LDAB**, and it uses the **IMM** addressing mode. Thus, the two bytes **C6 05** is the op code for the instruction **LDAB #05**.
  - If the first byte is **\$18**, use Sheet 2 of Table A.2, and do the same thing. For example, **18 06** is a two byte instruction, the mnemonic is **ABA**, and it uses the **INH** addressing mode, so

there is no operand. Thus, the two bytes **18 06** is the op code for the instruction **ABA**.

- Indexed addressing mode is fairly complicated to disassemble. You need to use Table A.3 to determine the operand. For example, the op code **\$E6** indicates **LDAB indexed**, and may use two to four bytes (one to three bytes in addition to the op code). The postbyte **01** indicates that the operand is 0,1, which is **5-bit constant offset**, which takes only one additional byte. All 5-bit constant offset, pre and post increment and decrement, and register offset instructions use one additional byte. All **9-bit constant offset** instructions use two additional bytes, with the second byte holding 8 bits of the 9 bit offset. (**The 9th bit is a direction bit**, which is held in the first postbyte.) All 16-bit constant offset instructions use three postbytes, with the 2nd and 3rd holding the 16-bit unsigned offset.

– Transfer (**TFR**) and exchange (**EXG**) instructions all have the op code **\$B7**. Use Table A.5 to determine whether it is **TFR** or an **EXG**, and to determine which registers are being used. If the most significant bit of the postbyte is **0**, **the instruction is a transfer instruction**.

- Loop instructions (Decrement and Branch, Increment and Branch, and Test and Branch) all have the op code **\$04**. To determine which instruction the op code **\$04** implies, and whether the branch is positive (forward) or negative (backward), use Table A.6. For example, in the sequence **04 35 EE**, the 04 indicates a loop instruction. The 35 indicates it is a **DBNE X** instruction (decrement register X and branch if

result is not equal to zero), and the direction is backward (negative). The **EE** indicates a branch of -18 bytes.

-

- Use up all the bytes for one instruction, then go on to the next instruction.

<b>C6 05</b>	<b>⇒ LDAB #\$05</b>	two-byte LDAB, IMM addressing mode
<b>CE 20 00</b>	<b>⇒ LDX #\$2000</b>	three-byte LDX, IMM addressing mode
<b>E6 01</b>	<b>⇒ LDAB 1,X</b>	two to four-byte LDAB, IDX addressing mode. Operand 01 => 1,X, a 5b constant offset which uses only one postbyte
<b>18 06</b>	<b>⇒ ABA</b>	two-byte ABA, INH addressing mode
<b>04 35 EE</b>	<b>⇒ DBNE X,(-18)</b>	three-byte loop instruction Postbyte 35 indicates DBNE X, negative
<b>3F</b>	<b>⇒ SWI</b>	one-byte SWI, INH addressing mode





**Table A-2. CPU12 Opcode Map (Sheet 2 of 2)**

00	MOVW	4	10	12	20	4	30	10	40	10	50	10	60	10	70	10	80	10	90	10	A0	10	B0	10	C0	10	D0	10	E0	10	F0	10	
IM-ID	5	IH	2	RL	4	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP
01	MOVW	5	11	12	21	3	31	10	41	10	51	10	61	10	71	10	81	10	91	10	A1	10	B1	10	C1	10	D1	10	E1	10	F1	10	
EX-ID	5	IH	2	RL	4	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP
02	MOVW	5	12	13	22	4/3	32	10	42	10	52	10	62	10	72	10	82	10	92	10	A2	10	B2	10	C2	10	D2	10	E2	10	F2	10	
ID-ID	4	EMACS	4	SP	4	RL	4	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP		
03	MOVW	5	13	3	23	4/3	33	10	43	10	53	10	63	10	73	10	83	10	93	10	A3	10	B3	10	C3	10	D3	10	E3	10	F3	10	
IM-EX	8	IH	2	RL	4	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP
04	MOVW	8	14	12	24	4/3	34	10	44	10	54	10	64	10	74	10	84	10	94	10	A4	10	B4	10	C4	10	D4	10	E4	10	F4	10	
EX-EX	8	IH	2	RL	4	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP
05	MOVW	5	15	12	25	4/3	35	10	45	10	55	10	65	10	75	10	85	10	95	10	A5	10	B5	10	C5	10	D5	10	E5	10	F5	10	
ID-EX	5	IH	2	RL	4	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP
06	ABA	2	16	2	26	4/3	36	10	46	10	56	10	66	10	76	10	86	10	96	10	A6	10	B6	10	C6	10	D6	10	E6	10	F6	10	
IH	2	SBA	2	RL	4	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP
07	DAA	3	17	2	27	4/3	37	10	47	10	57	10	67	10	77	10	87	10	97	10	A7	10	B7	10	C7	10	D7	10	E7	10	F7	10	
IH	2	CBA	2	RL	4	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP
08	MOVW	4	18	4-7	28	4/3	38	10	48	10	58	10	68	10	78	10	88	10	98	10	A8	10	B8	10	C8	10	D8	10	E8	10	F8	10	
IM-ID	4	ID	3-5	MAXA	4	LBVC	4	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP		
09	MOVW	5	19	4-7	29	4/3	39	10	49	10	59	10	69	10	79	10	89	10	99	10	A9	10	B9	10	C9	10	D9	10	E9	10	F9	10	
EX-ID	5	ID	3-5	MINA	4	LBVS	4	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP		
0A	MOVW	5	1A	4-7	2A	4/3	3A	†3n	4A	10	5A	10	6A	10	7A	10	8A	10	9A	10	AA	10	BA	10	CA	10	DA	10	EA	10	FA	10	
ID-ID	4	ID	3-5	EMAXD	4	LBPL	4	REV	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP		
0B	MOVW	4	1B	4-7	2B	4/3	3B	†5n/3n	4B	10	5B	10	6B	10	7B	10	8B	10	9B	10	AB	10	BB	10	CB	10	DB	10	EB	10	FB	10	
IM-EX	5	ID	3-5	EMIND	4	LBMI	4	REVW	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP		
0C	MOVW	6	1C	4-7	2C	4/3	3C	†7B	4C	10	5C	10	6C	10	7C	10	8C	10	9C	10	AC	10	BC	10	CC	10	DC	10	EC	10	FC	10	
EX-EX	6	ID	3-5	MAXM	4	LBGE	4	WAV	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP		
0D	MOVW	5	1D	D4-7	2D	4/3	3D	†6	4D	10	5D	10	6D	10	7D	10	8D	10	9D	10	AD	10	BD	10	CD	10	DD	10	ED	10	FD	10	
ID-EX	5	ID	3-5	MINM	4	LBLT	4	TBL	3	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP		
0E	TAB	2	1E	4-7	2E	4/3	3E	†8	4E	10	5E	10	6E	10	7E	10	8E	10	9E	10	AE	10	BE	10	CE	10	DE	10	EE	10	FE	10	
IH	2	ID	3-5	EMAXM	4	LBGT	4	STOP	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP		
0F	TBA	2	1F	4-7	2F	4/3	3F	10	4F	10	5F	10	6F	10	7F	10	8F	10	9F	10	AF	10	BF	10	CF	10	DF	10	EF	10	FF	10	
IH	2	ID	3-5	EMINM	4	LBLE	4	ETBL	3	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP	IH	2	TRAP	TRAP		

\* The opcode \$04 (on sheet 1 of 2) corresponds to one of the loop primitive instructions DBEQ, DBNE, IBEQ, IBNE, TBEQ, or TBNE.

† Refer to instruction summary for more information.

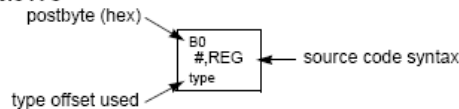
‡ Refer to instruction summary for different HC12 cycle count.

Page 2: When the CPU encounters a page 2 opcode (\$18 on page 1 of the opcode map), it treats the next byte of object code as a page 2 instruction opcode.

**Table A-3. Indexed Addressing Mode Postbyte Encoding (xb)**

00	0,X 5b const	10	-16,X 5b const	20	1,+X pre-inc	30	1,X+ post-inc	40	0,Y 5b const	50	-16,Y 5b const	60	1,+Y pre-inc	70	1,Y+ post-inc	80	0,SP 5b const	90	-16,SP 5b const	A0	1,+SP pre-inc	B0	1,SP+ post-inc	C0	0,PC 5b const	D0	-16,PC 5b const	E0	n,X 9b const	F0	n,SP 9b const
01	1,X 5b const	11	-15,X 5b const	21	2,+X pre-inc	31	2,X+ post-inc	41	1,Y 5b const	51	-15,Y 5b const	61	2,+Y pre-inc	71	2,Y+ post-inc	81	1,SP 5b const	91	-15,SP 5b const	A1	2,+SP pre-inc	B1	2,SP+ post-inc	C1	1,PC 5b const	D1	-15,PC 5b const	E1	-n,X 9b const	F1	-n,SP 9b const
02	2,X 5b const	12	-14,X 5b const	22	3,+X pre-inc	32	3,X+ post-inc	42	2,Y 5b const	52	-14,Y 5b const	62	3,+Y pre-inc	72	3,Y+ post-inc	82	2,SP 5b const	92	-14,SP 5b const	A2	3,+SP pre-inc	B2	3,SP+ post-inc	C2	2,PC 5b const	D2	-14,PC 5b const	E2	n,X 16b const	F2	n,SP 16b const
03	3,X 5b const	13	-13,X 5b const	23	4,+X pre-inc	33	4,X+ post-inc	43	3,Y 5b const	53	-13,Y 5b const	63	4,+Y pre-inc	73	4,Y+ post-inc	83	3,SP 5b const	93	-13,SP 5b const	A3	4,+SP pre-inc	B3	4,SP+ post-inc	C3	3,PC 5b const	D3	-13,PC 5b const	E3	[n,X] 16b indir	F3	[n,SP] 16b indir
04	4,X 5b const	14	-12,X 5b const	24	5,+X pre-inc	34	5,X+ post-inc	44	4,Y 5b const	54	-12,Y 5b const	64	5,+Y pre-inc	74	5,Y+ post-inc	84	4,SP 5b const	94	-12,SP 5b const	A4	5,+SP pre-inc	B4	5,SP+ post-inc	C4	4,PC 5b const	D4	-12,PC 5b const	E4	A,X A offset	F4	A,SP A offset
05	5,X 5b const	15	-11,X 5b const	25	6,+X pre-inc	35	6,X+ post-inc	45	5,Y 5b const	55	-11,Y 5b const	65	6,+Y pre-inc	75	6,Y+ post-inc	85	5,SP 5b const	95	-11,SP 5b const	A5	6,+SP pre-inc	B5	6,SP+ post-inc	C5	5,PC 5b const	D5	-11,PC 5b const	E5	B,X B offset	F5	B,SP B offset
06	6,X 5b const	16	-10,X 5b const	26	7,+X pre-inc	36	7,X+ post-inc	46	6,Y 5b const	56	-10,Y 5b const	66	7,+Y pre-inc	76	7,Y+ post-inc	86	6,SP 5b const	96	-10,SP 5b const	A6	7,+SP pre-inc	B6	7,SP+ post-inc	C6	6,PC 5b const	D6	-10,PC 5b const	E6	D,X D offset	F6	D,SP D offset
07	7,X 5b const	17	-9,X 5b const	27	8,+X pre-inc	37	8,X+ post-inc	47	7,Y 5b const	57	-9,Y 5b const	67	8,+Y pre-inc	77	8,Y+ post-inc	87	7,SP 5b const	97	-9,SP 5b const	A7	8,+SP pre-inc	B7	8,SP+ post-inc	C7	7,PC 5b const	D7	-9,PC 5b const	E7	[D,X] D indirect	F7	[D,SP] D indirect
08	8,X 5b const	18	-8,X 5b const	28	8,-X pre-dec	38	8,X- post-dec	48	8,Y 5b const	58	-8,Y 5b const	68	8,-Y pre-dec	78	8,Y- post-dec	88	8,SP 5b const	98	-8,SP 5b const	A8	8,-SP pre-dec	B8	8,SP- post-dec	C8	8,PC 5b const	D8	-8,PC 5b const	E8	n,Y 9b const	F8	n,PC 9b const
09	9,X 5b const	19	-7,X 5b const	29	7,-X pre-dec	39	7,X- post-dec	49	9,Y 5b const	59	-7,Y 5b const	69	7,-Y pre-dec	79	7,Y- post-dec	89	9,SP 5b const	99	-7,SP 5b const	A9	7,-SP pre-dec	B9	7,SP- post-dec	C9	9,PC 5b const	D9	-7,PC 5b const	E9	-n,Y 9b const	F9	-n,PC 9b const
0A	10,X 5b const	1A	-6,X 5b const	2A	8,-X pre-dec	3A	8,X- post-dec	4A	10,Y 5b const	5A	-6,Y 5b const	6A	8,-Y pre-dec	7A	8,Y- post-dec	8A	10,SP 5b const	9A	-6,SP 5b const	AA	8,-SP pre-dec	BA	8,SP- post-dec	CA	10,PC 5b const	DA	-6,PC 5b const	EA	n,Y 16b const	FA	n,PC 16b const
0B	11,X 5b const	1B	-5,X 5b const	2B	5,-X pre-dec	3B	5,X- post-dec	4B	11,Y 5b const	5B	-5,Y 5b const	6B	5,-Y pre-dec	7B	5,Y- post-dec	8B	11,SP 5b const	9B	-5,SP 5b const	AB	5,-SP pre-dec	BB	5,SP- post-dec	CB	11,PC 5b const	DB	-5,PC 5b const	EB	[n,Y] 16b indir	FB	[n,PC] 16b indir
0C	12,X 5b const	1C	-4,X 5b const	2C	4,-X pre-dec	3C	4,X- post-dec	4C	12,Y 5b const	5C	-4,Y 5b const	6C	4,-Y pre-dec	7C	4,Y- post-dec	8C	12,SP 5b const	9C	-4,SP 5b const	AC	4,-SP pre-dec	BC	4,SP- post-dec	CC	12,PC 5b const	DC	-4,PC 5b const	EC	A,Y A offset	FC	A,PC A offset
0D	13,X 5b const	1D	-3,X 5b const	2D	3,-X pre-dec	3D	3,X- post-dec	4D	13,Y 5b const	5D	-3,Y 5b const	6D	3,-Y pre-dec	7D	3,Y- post-dec	8D	13,SP 5b const	9D	-3,SP 5b const	AD	3,-SP pre-dec	BD	3,SP- post-dec	CD	13,PC 5b const	DD	-3,PC 5b const	ED	B,Y B offset	FD	B,PC B offset
0E	14,X 5b const	1E	-2,X 5b const	2E	2,-X pre-dec	3E	2,X- post-dec	4E	14,Y 5b const	5E	-2,Y 5b const	6E	2,-Y pre-dec	7E	2,Y- post-dec	8E	14,SP 5b const	9E	-2,SP 5b const	AE	2,-SP pre-dec	BE	2,SP- post-dec	CE	14,PC 5b const	DE	-2,PC 5b const	EE	D,Y D offset	FE	D,PC D offset
0F	15,X 5b const	1F	-1,X 5b const	2F	1,-X pre-dec	3F	1,X- post-dec	4F	15,Y 5b const	5F	-1,Y 5b const	6F	1,-Y pre-dec	7F	1,Y- post-dec	8F	15,SP 5b const	9F	-1,SP 5b const	AF	1,-SP pre-dec	BF	1,SP- post-dec	CF	16,PC 5b const	DF	-1,PC 5b const	EF	[D,Y] D indirect	FF	[D,PC] D indirect

**Key to Table A-3**



**Table A-5. Transfer and Exchange Postbyte Encoding**

TRANSFERS									
↓LS	MS⇒	0	1	2	3	4	5	6	7
0		A ⇒ A	B ⇒ A	CCR ⇒ A	TMP3 <sub>L</sub> ⇒ A	B ⇒ A	X <sub>L</sub> ⇒ A	Y <sub>L</sub> ⇒ A	SP <sub>L</sub> ⇒ A
1		A ⇒ B	B ⇒ B	CCR ⇒ B	TMP3 <sub>L</sub> ⇒ B	B ⇒ B	X <sub>L</sub> ⇒ B	Y <sub>L</sub> ⇒ B	SP <sub>L</sub> ⇒ B
2		A ⇒ CCR	B ⇒ CCR	CCR ⇒ CCR	TMP3 <sub>L</sub> ⇒ CCR	B ⇒ CCR	X <sub>L</sub> ⇒ CCR	Y <sub>L</sub> ⇒ CCR	SP <sub>L</sub> ⇒ CCR
3		sex:A ⇒ TMP2	sex:B ⇒ TMP2	sex:CCR ⇒ TMP2	TMP3 ⇒ TMP2	D ⇒ TMP2	X ⇒ TMP2	Y ⇒ TMP2	SP ⇒ TMP2
4		sex:A ⇒ D SEX A,D	sex:B ⇒ D SEX B,D	sex:CCR ⇒ D SEX CCR,D	TMP3 ⇒ D	D ⇒ D	X ⇒ D	Y ⇒ D	SP ⇒ D
5		sex:A ⇒ X SEX A,X	sex:B ⇒ X SEX B,X	sex:CCR ⇒ X SEX CCR,X	TMP3 ⇒ X	D ⇒ X	X ⇒ X	Y ⇒ X	SP ⇒ X
6		sex:A ⇒ Y SEX A,Y	sex:B ⇒ Y SEX B,Y	sex:CCR ⇒ Y SEX CCR,Y	TMP3 ⇒ Y	D ⇒ Y	X ⇒ Y	Y ⇒ Y	SP ⇒ Y
7		sex:A ⇒ SP SEX A,SP	sex:B ⇒ SP SEX B,SP	sex:CCR ⇒ SP SEX CCR,SP	TMP3 ⇒ SP	D ⇒ SP	X ⇒ SP	Y ⇒ SP	SP ⇒ SP
EXCHANGES									
↓LS	MS⇒	8	9	A	B	C	D	E	F
0		A ⇔ A	B ⇔ A	CCR ⇔ A	TMP3 <sub>L</sub> ⇔ A \$00:A ⇔ TMP3	B ⇔ A A ⇔ B	X <sub>L</sub> ⇔ A \$00:A ⇔ X	Y <sub>L</sub> ⇔ A \$00:A ⇔ Y	SP <sub>L</sub> ⇔ A \$00:A ⇔ SP
1		A ⇔ B	B ⇔ B	CCR ⇔ B	TMP3 <sub>L</sub> ⇔ B \$FF:B ⇔ TMP3	B ⇔ B \$FF ⇔ A	X <sub>L</sub> ⇔ B \$FF:B ⇔ X	Y <sub>L</sub> ⇔ B \$FF:B ⇔ Y	SP <sub>L</sub> ⇔ B \$FF:B ⇔ SP
2		A ⇔ CCR	B ⇔ CCR	CCR ⇔ CCR	TMP3 <sub>L</sub> ⇔ CCR \$FF:CCR ⇔ TMP3	B ⇔ CCR \$FF:CCR ⇔ D	X <sub>L</sub> ⇔ CCR \$FF:CCR ⇔ X	Y <sub>L</sub> ⇔ CCR \$FF:CCR ⇔ Y	SP <sub>L</sub> ⇔ CCR \$FF:CCR ⇔ SP
3		\$00:A ⇔ TMP2 TMP2 <sub>L</sub> ⇔ A	\$00:B ⇔ TMP2 TMP2 <sub>L</sub> ⇔ B	\$00:CCR ⇔ TMP2 TMP2 <sub>L</sub> ⇔ CCR	TMP3 ⇔ TMP2	D ⇔ TMP2	X ⇔ TMP2	Y ⇔ TMP2	SP ⇔ TMP2
4		\$00:A ⇔ D	\$00:B ⇔ D	\$00:CCR ⇔ D B ⇔ CCR	TMP3 ⇔ D	D ⇔ D	X ⇔ D	Y ⇔ D	SP ⇔ D
5		\$00:A ⇔ X X <sub>L</sub> ⇔ A	\$00:B ⇔ X X <sub>L</sub> ⇔ B	\$00:CCR ⇔ X X <sub>L</sub> ⇔ CCR	TMP3 ⇔ X	D ⇔ X	X ⇔ X	Y ⇔ X	SP ⇔ X
6		\$00:A ⇔ Y Y <sub>L</sub> ⇔ A	\$00:B ⇔ Y Y <sub>L</sub> ⇔ B	\$00:CCR ⇔ Y Y <sub>L</sub> ⇔ CCR	TMP3 ⇔ Y	D ⇔ Y	X ⇔ Y	Y ⇔ Y	SP ⇔ Y
7		\$00:A ⇔ SP SP <sub>L</sub> ⇔ A	\$00:B ⇔ SP SP <sub>L</sub> ⇔ B	\$00:CCR ⇔ SP SP <sub>L</sub> ⇔ CCR	TMP3 ⇔ SP	D ⇔ SP	X ⇔ SP	Y ⇔ SP	SP ⇔ SP

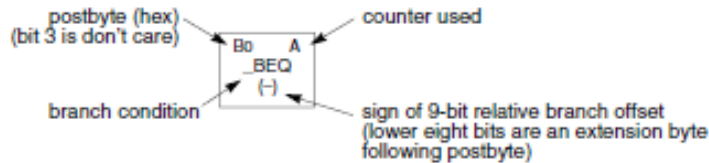
TMP2 and TMP3 registers are for factory use only.



**Table A-6. Loop Primitive Postbyte Encoding (1b)**

00	A	DBEQ (+)	10	A	DBEQ (-)	20	A	DBNE (+)	30	A	DBNE (-)	40	A	TBEQ (+)	50	A	TBEQ (-)	60	A	TBNE (+)	70	A	TBNE (-)	80	A	IBEQ (+)	90	A	IBEQ (-)	A0	A	IBNE (+)	B0	A	IBNE (-)
01	B	DBEQ (+)	11	B	DBEQ (-)	21	B	DBNE (+)	31	B	DBNE (-)	41	B	TBEQ (+)	51	B	TBEQ (-)	61	B	TBNE (+)	71	B	TBNE (-)	81	B	IBEQ (+)	91	B	IBEQ (-)	A1	B	IBNE (+)	B1	B	IBNE (-)
02		—	12		—	22		—	32		—	42		—	52		—	62		—	72		—	82		—	92		—	A2		—	B2		—
03		—	13		—	23		—	33		—	43		—	53		—	63		—	73		—	83		—	93		—	A3		—	B3		—
04	D	DBEQ (+)	14	D	DBEQ (-)	24	D	DBNE (+)	34	D	DBNE (-)	44	D	TBEQ (+)	54	D	TBEQ (-)	64	D	TBNE (+)	74	D	TBNE (-)	84	D	IBEQ (+)	94	D	IBEQ (-)	A4	D	IBNE (+)	B4	D	IBNE (-)
05	X	DBEQ (+)	15	X	DBEQ (-)	25	X	DBNE (+)	35	X	DBNE (-)	45	X	TBEQ (+)	55	X	TBEQ (-)	65	X	TBNE (+)	75	X	TBNE (-)	85	X	IBEQ (+)	95	X	IBEQ (-)	A5	X	IBNE (+)	B5	X	IBNE (-)
06	Y	DBEQ (+)	16	Y	DBEQ (-)	26	Y	DBNE (+)	36	Y	DBNE (-)	46	Y	TBEQ (+)	56	Y	TBEQ (-)	66	Y	TBNE (+)	76	Y	TBNE (-)	86	Y	IBEQ (+)	96	Y	IBEQ (-)	A6	Y	IBNE (+)	B6	Y	IBNE (-)
07	SP	DBEQ (+)	17	SP	DBEQ (-)	27	SP	DBNE (+)	37	SP	DBNE (-)	47	SP	TBEQ (+)	57	SP	TBEQ (-)	67	SP	TBNE (+)	77	SP	TBNE (-)	87	SP	IBEQ (+)	97	SP	IBEQ (-)	A7	SP	IBNE (+)	B7	SP	IBNE (-)

**Key to Table A-6**



**Table A-7. Branch/Complementary Branch**

Branch				Complementary Branch			
Test	Mnemonic	Opcode	Boolean	Test	Mnemonic	Opcode	Comment
r>m	BGT	2E	$Z + (N \oplus V) = 0$	r≤m	BLE	2F	Signed
r≥m	BGE	2C	$N \oplus V = 0$	r<m	BLT	2D	Signed
r=m	BEQ	27	$Z = 1$	r≠m	BNE	26	Signed
r≤m	BLE	2F	$Z + (N \oplus V) = 1$	r>m	BGT	2E	Signed
r<m	BLT	2D	$N \oplus V = 1$	r≥m	BGE	2C	Signed
r>m	BHI	22	$C + Z = 0$	r≤m	BLS	23	Unsigned
r≥m	BHS/BCC	24	$C = 0$	r<m	BLO/BCS	25	Unsigned
r=m	BEQ	27	$Z = 1$	r≠m	BNE	26	Unsigned
r≤m	BLS	23	$C + Z = 1$	r>m	BHI	22	Unsigned
r<m	BLO/BCS	25	$C = 1$	r≥m	BHS/BCC	24	Unsigned
Carry	BCS	25	$C = 1$	No Carry	BCC	24	Simple
Negative	BMI	2B	$N = 1$	Plus	BPL	2A	Simple
Overflow	BVS	29	$V = 1$	No Overflow	BVC	28	Simple
r=0	BEQ	27	$Z = 1$	r≠0	BNE	26	Simple
Always	BRA	20	—	Never	BRN	21	Unconditional

For 16-bit offset long branches precede opcode with a \$18 page prebyte.