

# CIC filters

By

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# Overview

- Over-Sampling and Averaging
- Effective Number of Bits(ENOB)
- Moving Average Filter
- Comb-Integrator Moving Average Filter
- Re-arranging to CIC filter
- Nth Order CIC filter
- Implementation
- Frequency Response of the CIC filter

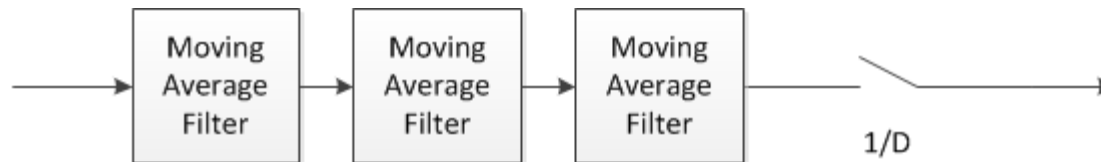
# Over-Sampling and Averaging

- Increases Bit resolution
- Increasing N bits out requires  $2^N$  samples
- Increasing Effective Number of Bits(ENOB)
  - $F_{os} = F_{out} * 2^{(2n)} \Rightarrow n = \log_4(F_{os}/F_{out}) = \log_4(D)$
- For 50MHz sampling and 16kHz output
  - $F_{os}/F_{out} = 3125$
  - 11.6 Bits out
  - 5.8 ENOB



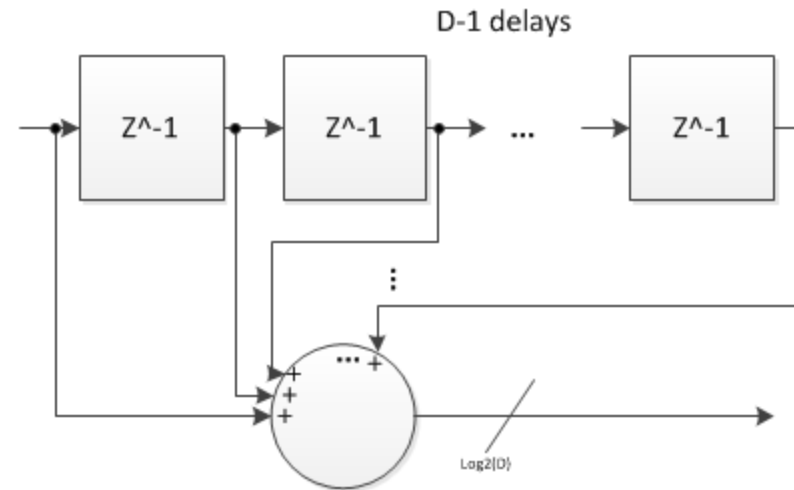
# Getting 16 ENOB

- Add 2 more averaging filters
  - Bit width =  $11.6 * 3 = 34.8$
  - ENOB =  $3 * 5.8 = 17.414$  bits
- Resource usage grows exponentially



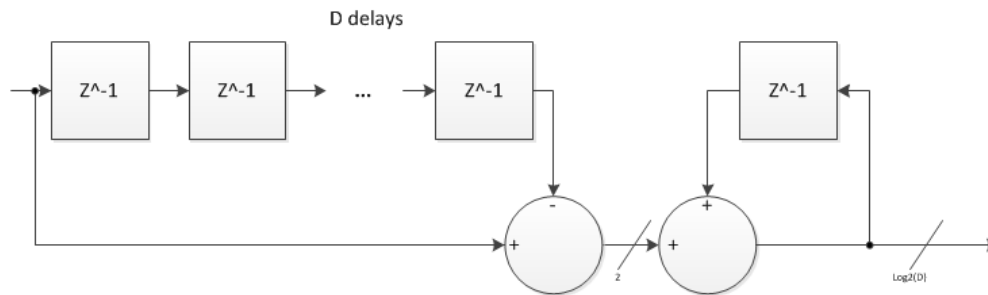
# Basic Moving Average w/ Gain

- Directly sums last D bits
  - $D \cdot \text{Bit\_width}$  of bits of storage
  - D adders
  - $\log_2(D)$  bits output latch for decimator
  - 3 averaging filters in series requires  $D + D \cdot \log_2(D) + D \cdot \log_2(D) \cdot 2$  bits of storage and  $3 \cdot D$  adders

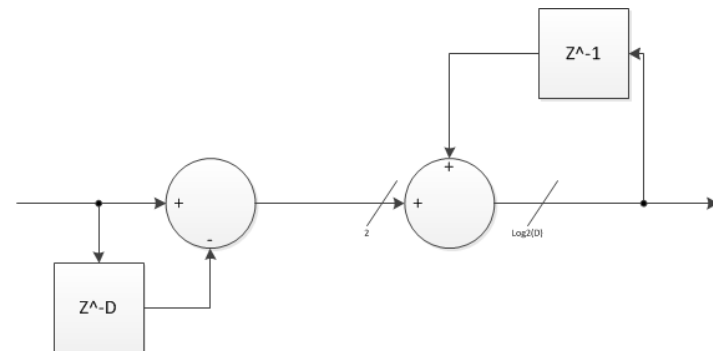


# Comb-Integrator Moving Average Filter

- Still needs same amount of storage
- Needs one adder/subtractor and one integrator

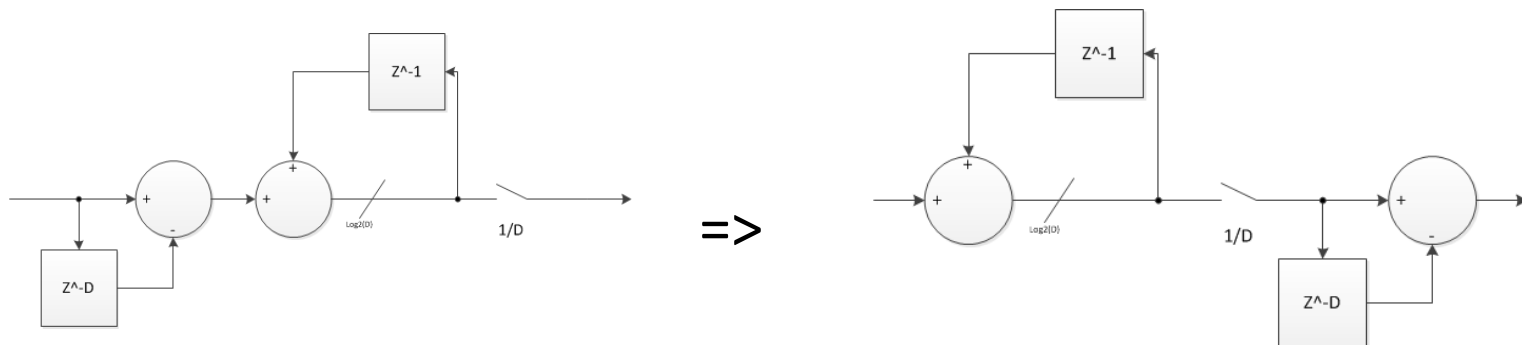


or



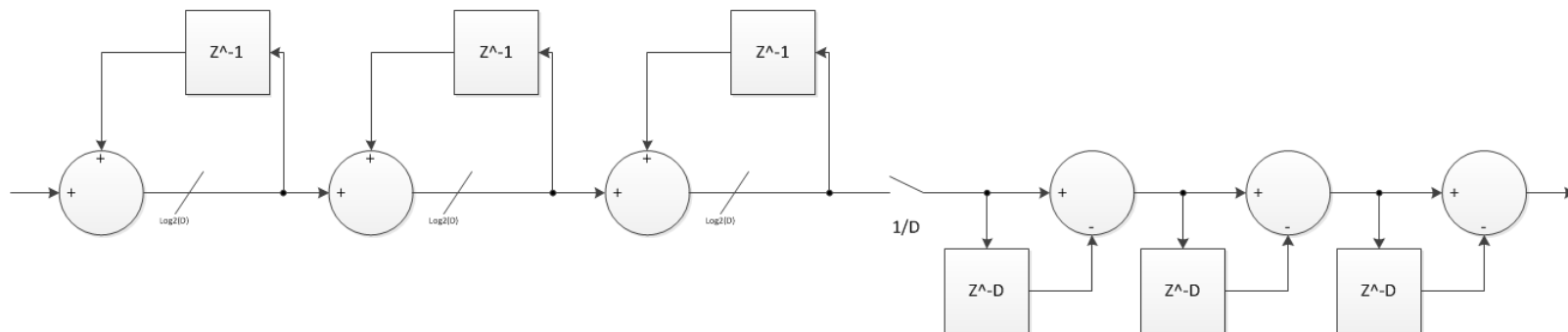
# Re-arrange LTI systems

- Integrate, then Decimate, then Comb
- If the Comb delay is the same as the decimation time, the delay  $D$  is the last sample from the decimator, reducing storage by a factor of  $D$



# Nth order Cascade Integrated Comb Filter

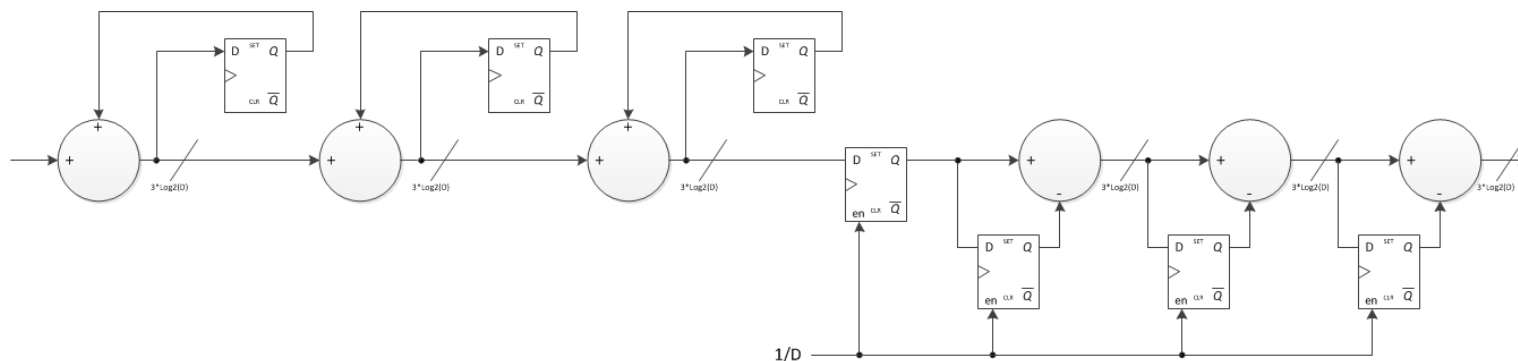
- Take  $N$  moving average filters in sequence with decimation at the end
  - Rearrange all integrators first, and comb filters last, with the decimator in the middle
- Integrator overflows are removed by combs if unsigned math is used and the bit width is at least  $N \cdot \log_2(D)$





# Implementation

- All logic runs on main clock
- All Integrators are always enabled
- Registers for the decimator and comb filters are enabled every Dth cycle ( $D=3125$ )
- Uses  $(2*N+1)*N*\log_2(D)$  bits of storage

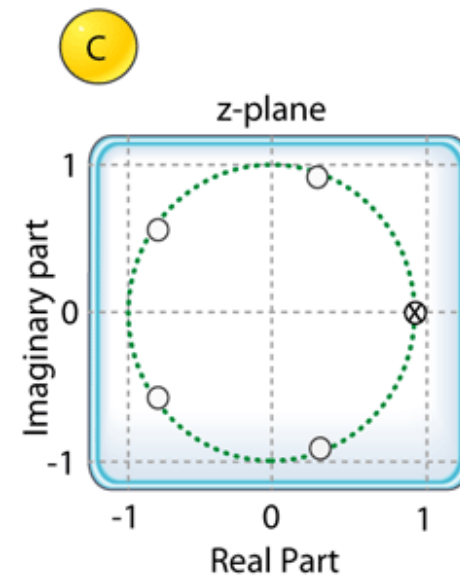
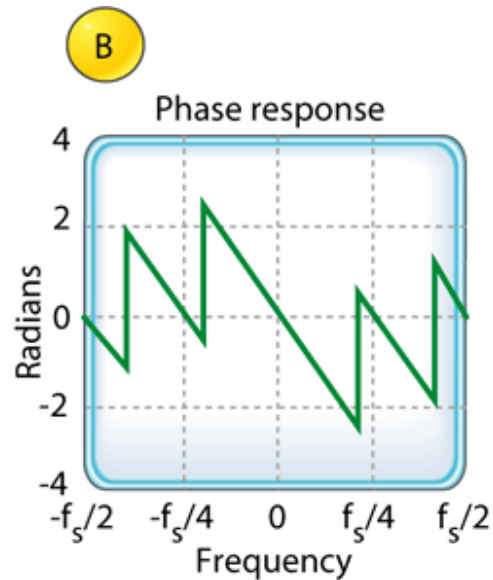
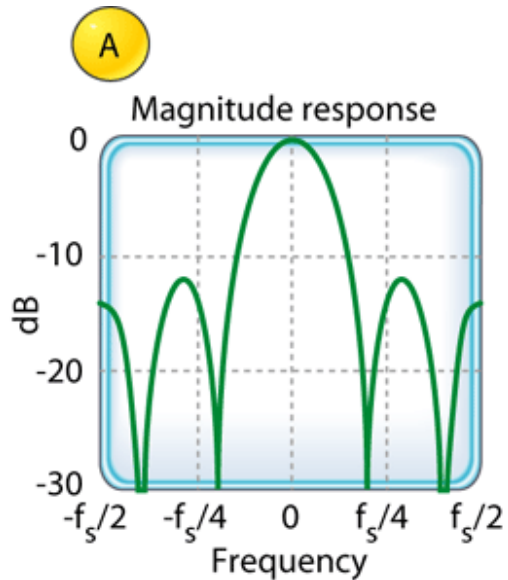


# Frequency Response

- Gain =  $\text{abs}(\sin(\pi * f * D) / \sin(\pi * f))^N$
- Phase is linear
- For 3<sup>rd</sup> order filter with 50MHz sample rate and 16kHz output rate
  - 3dB at 4250Hz
  - 11dB drop at 8kHz,
  - min 40dB suppression above 16kHz

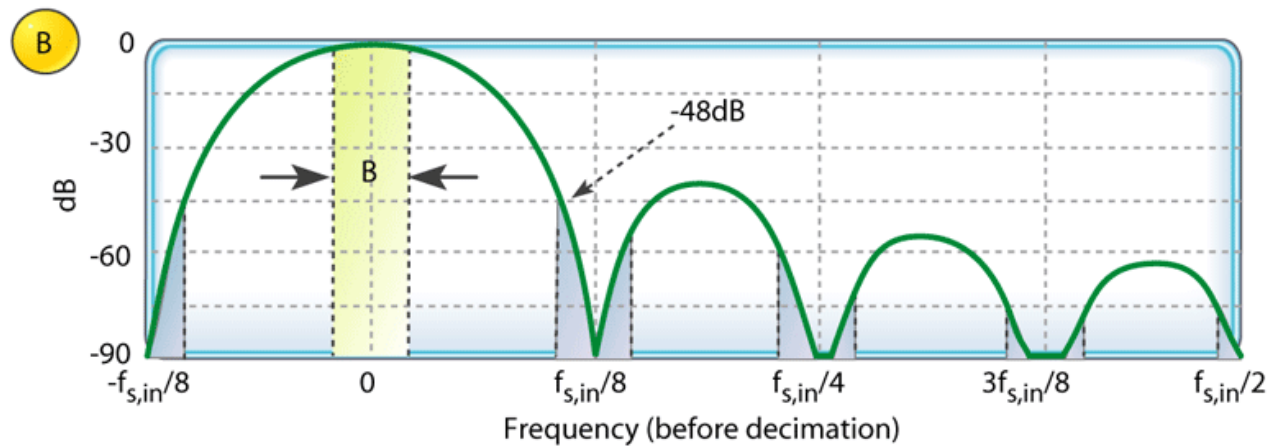
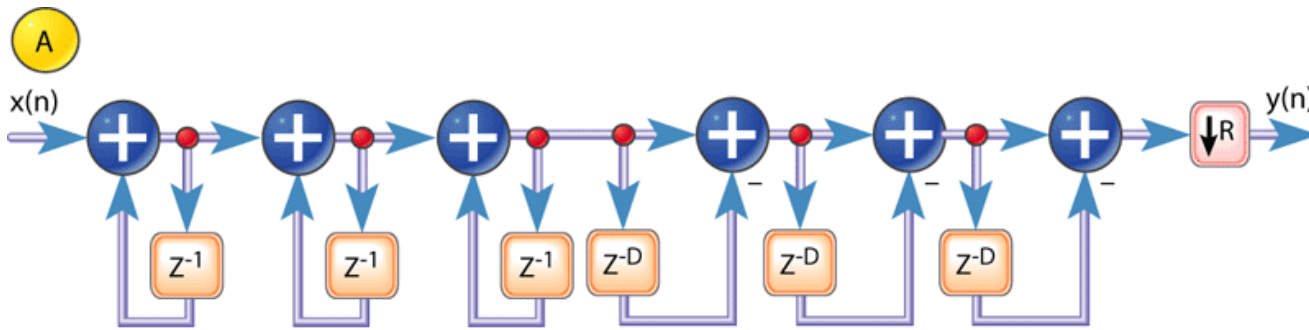
# Frequency Response

- 1<sup>st</sup> order CIC filter response
  - $D=8$



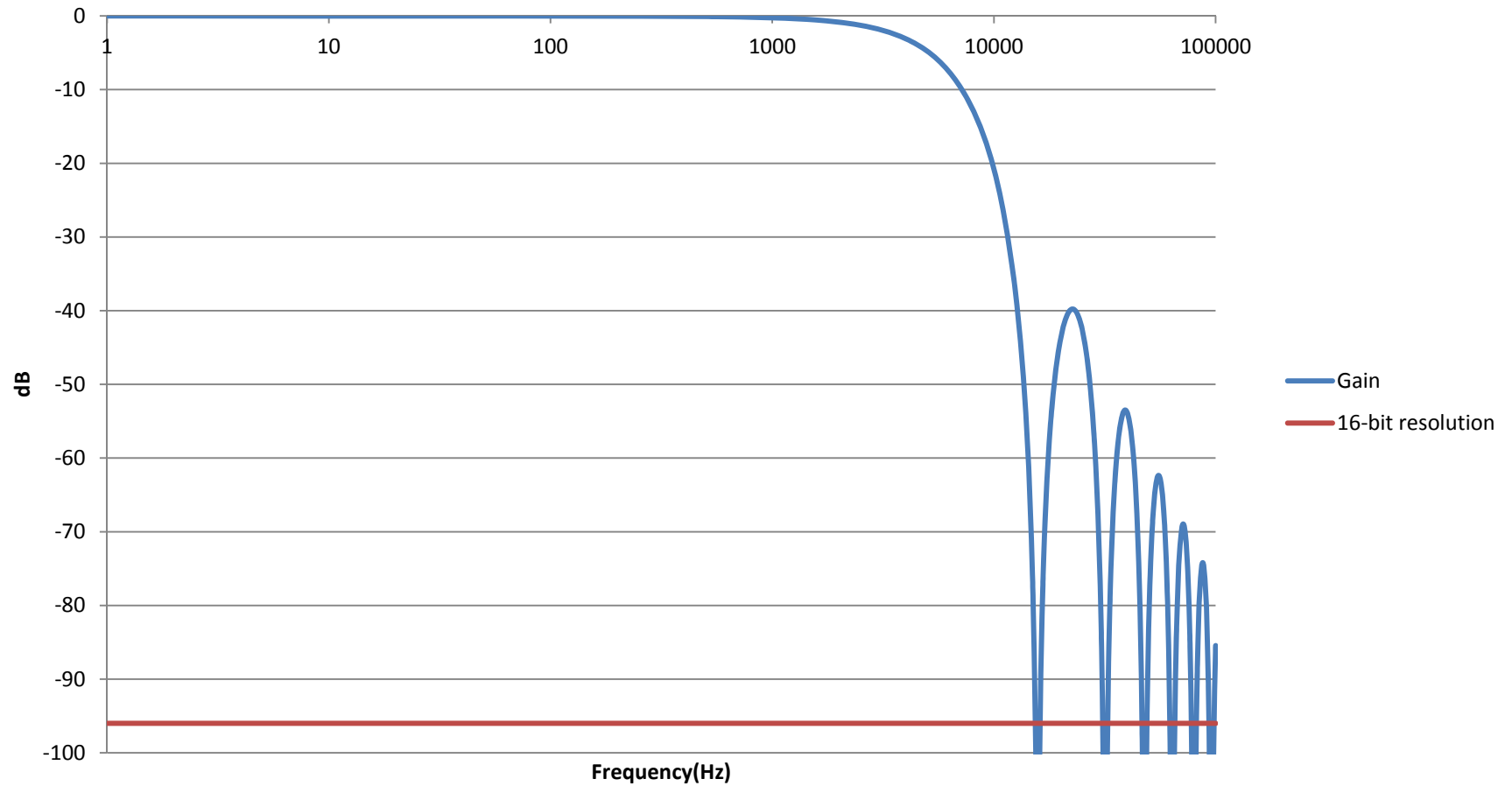
# Frequency Response

- 3<sup>rd</sup> order CIC filter frequency response
  - $D=R=8$



# Frequency Response

3<sup>rd</sup> Order CIC Gain 50MHz Sampling Rate D=3125



# References

- <http://www.embedded.com/design/configurable-systems/4006446/Understanding-cascaded-integrator-comb-filters>
- <http://dspguru.com/sites/dspguru/files/cic.pdf>
- <http://home.mit.bme.hu/~kollar/papers/cic.pdf>