Mid-term Project

The objective of this project is to implement an embedded control system on an Altera FPGA target board (DE0 or DE1). The modules of the digital control system are shown in Figure 1 (see also section 'The Structure of a Digital Control System', pages 2-6 in textbook). In this project the process is a DC motor and the controlled variable is the rotor speed. A reference speed can be input through the I/O or the JTAG ports. The Digital to Analog Converter (DAC) and Analog to Digital (ADC) devices interface the digital with the analog domain. These DAC will be substituted by a Pulse Width Modulation (PWM) subsystem which produces a voltage proportional to a frequency modulated signal, and the ADC is substituted by a digital encoder which produces digital pulses with a frequency proportional to the rotor speed. This process-sensor arrangement has been used in EE 308 (Microcontrollers).

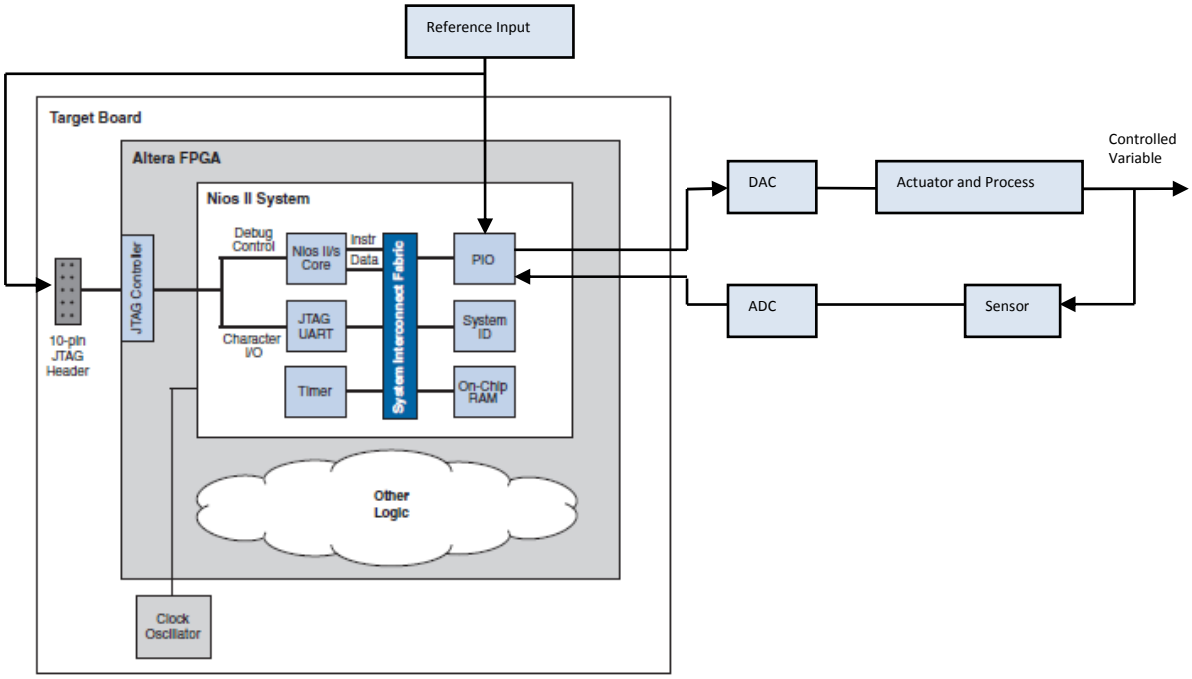

Figure 1. Block diagram of a digital control system.

The Altera FPGA development boards are located in the DSP/Controls Lab. We will implement a NIOS II System or a System on a Programmable Chip (SOPC) on this board using the Quartus II and NIOS II Embedded Design Suite software tools. We will implement a PID controller on the NIOS II System and observe the effect of different PID controller parameters and sampling intervals Ts, in the response of the process:

- Time constant τ.
- Rise time Tr
- Percent overshoot (PO)
- Peak time Tp
- Settling time Ts.

More details will be given in class.