EE 554 – Miniproject I

Introduction

Building embedded system in FPGAs is a broad subject, which involves systems requirements analysis, hardware design tasks, and software design tasks. In this assignment it is required that you develop a simple embedded system on an Altera board, following instructions outlined on the "Nios II Hardware Development Tutorial". The tutorial demonstrates a small Nios II system for control applications, which displays character I/O output and blinks LEDs in a binary counting pattern. This Nios II system can also communicate with a host computer, allowing the host computer to control logic inside the FPGA, as shown in Figure 1.

The example Nios II system contains the following:

- Nios II/s processor core
- On-chip memory
- Timer
- JTAG UART
- 8-bit parallel I/O (PIO) pins to control LEDs
- System identification component

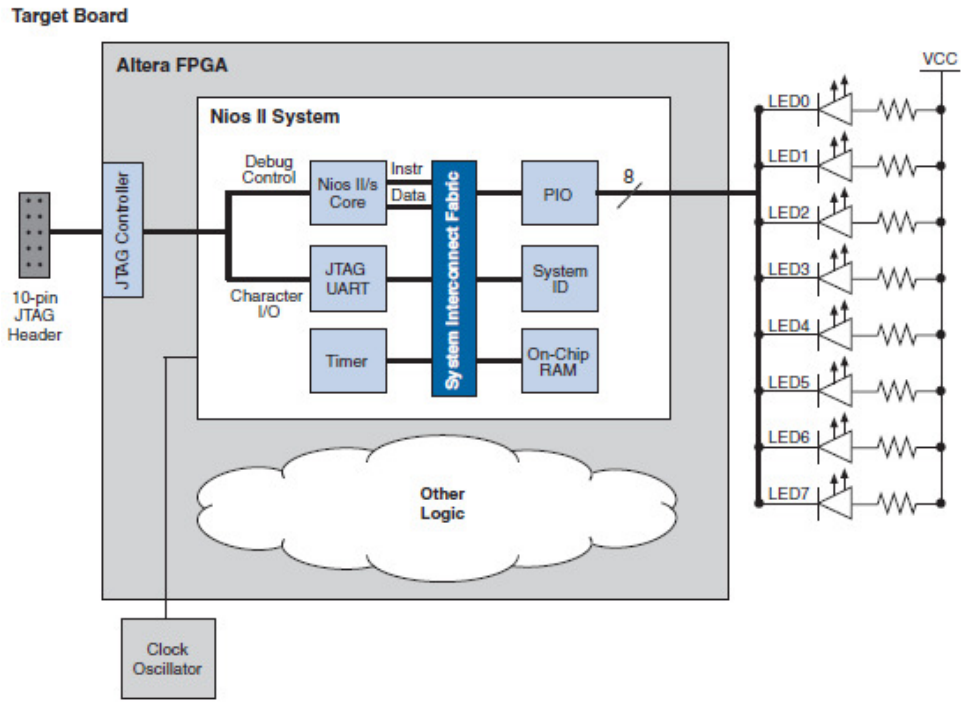

Figure 1. Block diagram of the embedded system (taken from Nios II Hardware Development Tutorial).

Software and Hardware Requirements

Use Quarus II and NIOS II Altera development platforms to implement the counter. Both, Quartus II and NIOS II platforms are installed in the DSP Lab. Also, we have available DE0 (and DE0-Nano boards) for the class. The boards should remain in the DSP/Control Lab at all times.

Documentation

You need to demonstrate the embedded system, and hand in a two-page report that may include, but is not limited to: names of participants, problems and solutions you encountered, concluding remarks (an electronic version is preferred).