AC Electrical Characteristics (V_{DD} = Min. to Max., Commercial and Industrial Temperature Ranges)

Symbol	Parameter	71V016SA10[2]		71V016SA12		71V016SA15		71V016SA20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	10	—	12	—	15	—	20	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	20	ns
t_{ACS}	Chip Select Access Time	—	10	—	12	—	15	—	20	ns
t_{CLZ}[1]	Chip Select Low to Output in Low-Z	4	—	4	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Select High to Output in High-Z	—	5	—	6	—	6	—	8	ns
t_{OE}	Output Enable Low to Output Valid	—	5	—	6	—	7	—	8	ns
t_{OLZ}[1]	Output Enable Low to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Enable High to Output in High-Z	—	5	—	6	—	6	—	8	ns
t_{OH}	Output Hold from Address Change	4	—	4	—	4	—	4	—	ns
t_{BE}	Byte Enable Low to Output Valid	—	5	—	6	—	7	—	8	ns
t_{BLZ}[1]	Byte Enable Low to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t_{BHZ}[1]	Byte Enable High to Output in High-Z	—	5	—	6	—	6	—	8	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	10	—	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End of Write	7	—	8	—	10	—	12	—	ns
t_{CW}	Chip Select Low to End of Write	7	—	8	—	10	—	12	—	ns
t_{BW}	Byte Enable Low to End of Write	7	—	8	—	10	—	12	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Address Hold from End of Write	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	7	—	8	—	10	—	12	—	ns
t_{DW}	Data Valid to End of Write	5	—	6	—	7	—	9	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Write Enable High to Output in Low-Z	3	—	3	—	3	—	3	—	ns
t_{WHZ}[1]	Write Enable Low to Output in High-Z	—	5	—	6	—	6	—	8	ns

NOTES:
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.
2. 0°C to +70°C temperature range only.

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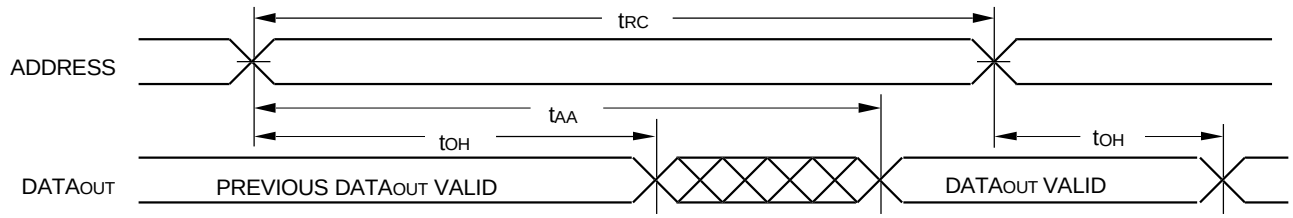
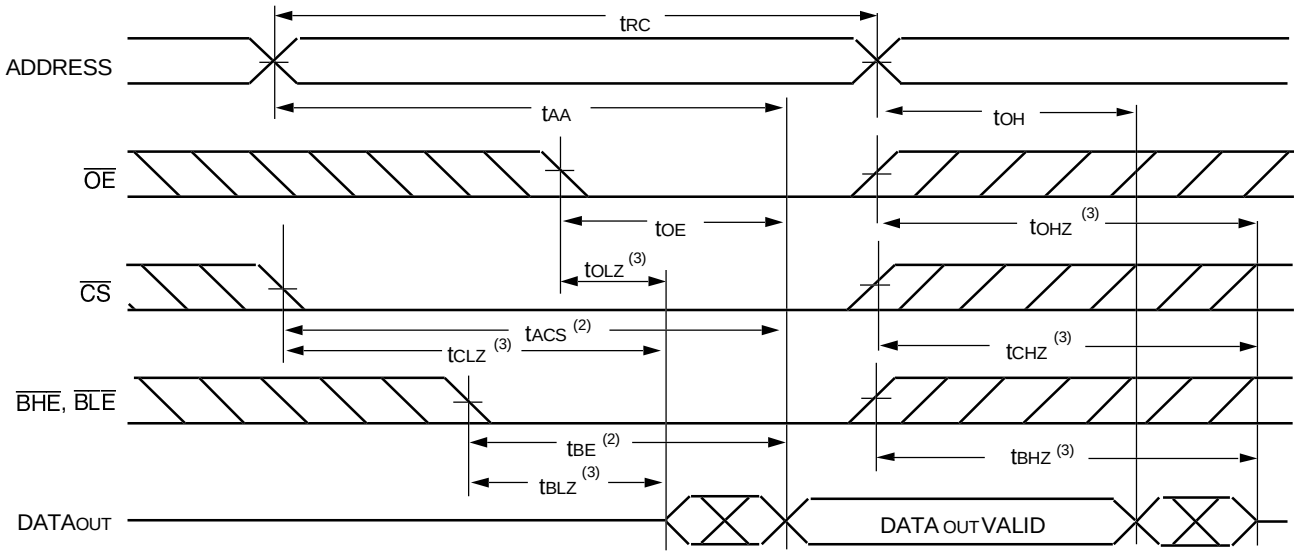
Timing Waveform of Read Cycle No. 1[1,2,3]



NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. $\overline{OE}$, $\overline{BHE}$, and $\overline{BLE}$ are LOW.

3834 drw 06

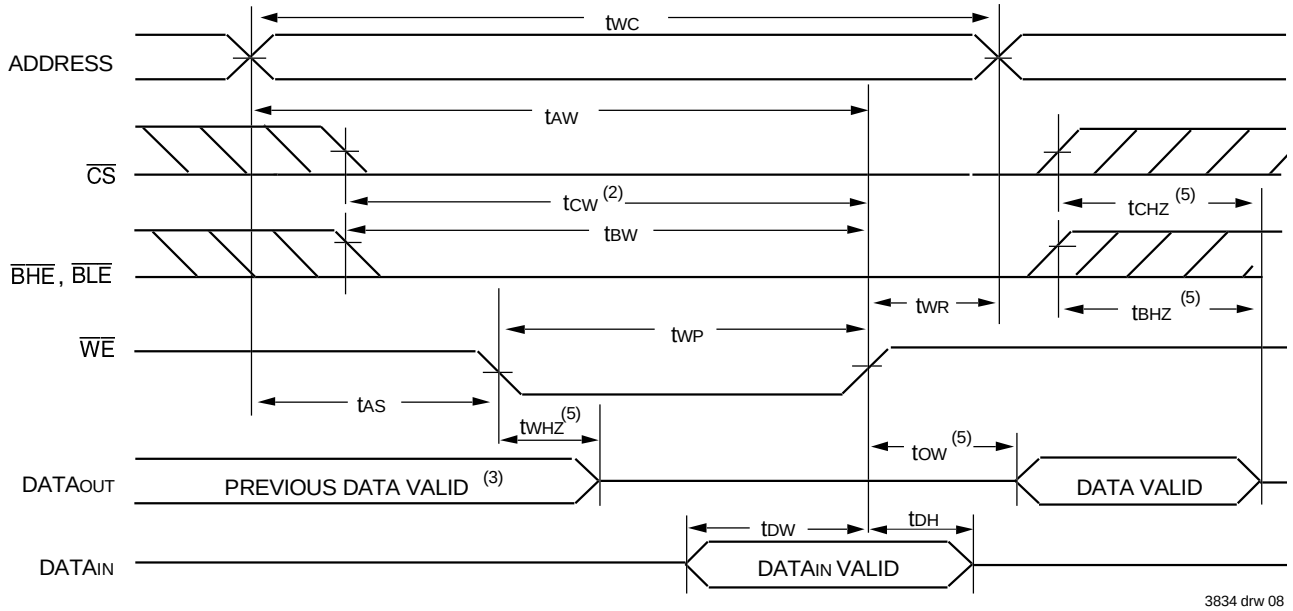
Timing Waveform of Read Cycle No. 2(1)



3834 drw 07

NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Address must be valid prior to or coincident with the later of $\overline{CS}$, $\overline{BHE}$, or $\overline{BLE}$ transition LOW; otherwise t_{AA} is the limiting parameter.
3. Transition is measured ±200mV from steady state.

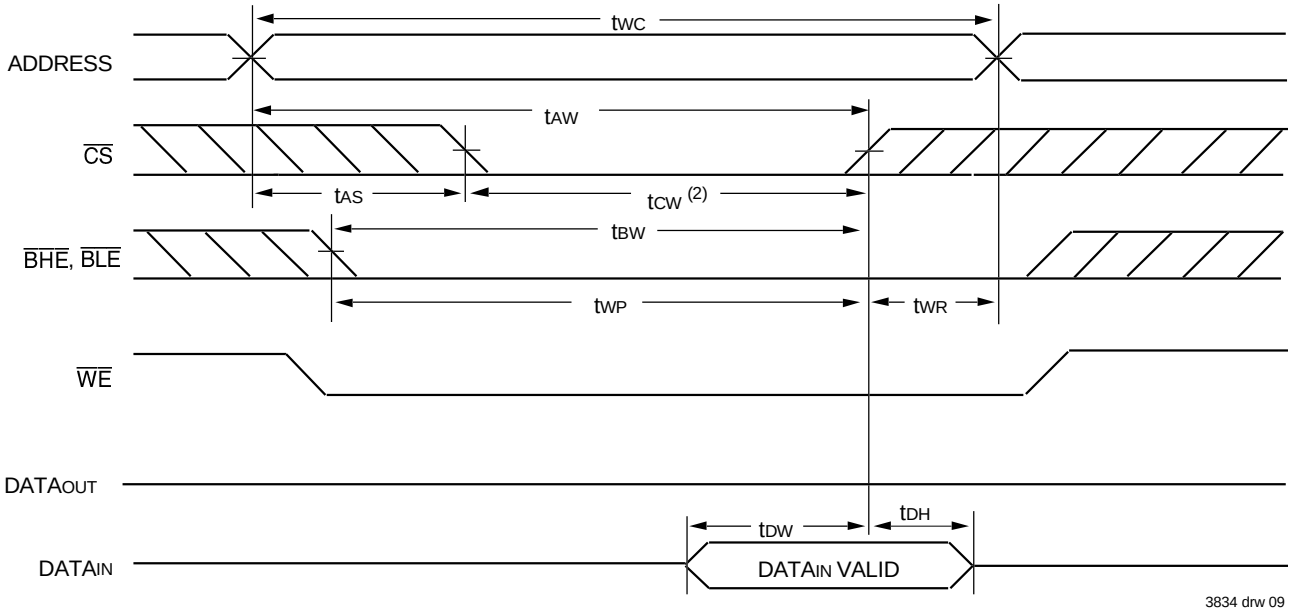
Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)(1,2,4)



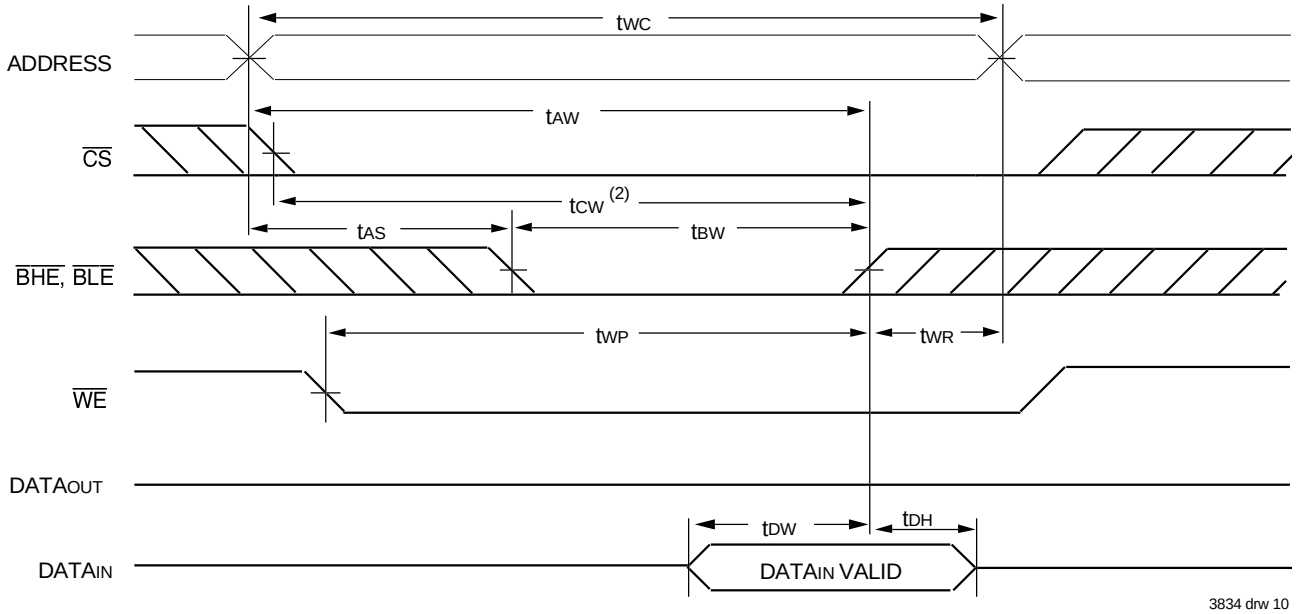
3834 drw 08

NOTES:
1. A write occurs during the overlap of a LOW $\overline{CS}$, LOW $\overline{BHE}$ or $\overline{BLE}$, and a LOW $\overline{WE}$.
2. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP}.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{CS}$ LOW or $\overline{BHE}$ and $\overline{BLE}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured ±200mV from steady state.

Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)(1,4)



Timing Waveform of Write Cycle No. 3 ($\overline{BHE}$, $\overline{BLE}$ Controlled Timing)(1,4)



NOTES:

1. A write occurs during the overlap of a LOW $\overline{CS}$, LOW $\overline{BHE}$ or $\overline{BLE}$, and a LOW $\overline{WE}$.
2. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP}.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{CS}$ LOW or $\overline{BHE}$ and $\overline{BLE}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured ±200mV from steady state.