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FIFTH EDITION

MICROELECTRONIC CIRCUITS

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Cover Illustration: The chip shown is an inside view of a mass-produced surface-micromachined gyroscope system, integrated on a 3mm by 3mm die, and using a standard 3-m 2-V BiCMOS process suited for the harsh automotive environment. This first single-chip gyroscopic sensor, in which micro-mechanical and electronic components are intimately entwined on the same chip, provides unprecedented performance through the use of a collection of precision-directed techniques, including emphasis on differential operation (both mechanically and electronically) bolstered by trimmable thin-film resistive components. This tiny, robust, low-power, angular-rate-to-voltage transducer, having a sensitivity of 12.5mV/°/s and resolution of 0.015°/s (or 50°/hour) has a myriad of applications—including automotive skid control and rollover detection, dead reckoning for GPS backup and robot motion control, and camera-field stabilization. The complete gyroscope package, weighing 1/3 gram with a volume of 1/6 cubic centimeter, uses 30mW from a 5-V supply. *Source:* John A. Geen, Steven J. Sherman, John F. Chang, Stephen R. Lewis; Single-chip surface micromachined integrated Gyroscope with 50°/h Allan deviation, IEEE Journal of Solid-State Circuits, vol. 37, pp. 1860–1866, December 2002. (Originally presented at ISSCC 2002.) Photographed by John Chang, provided by John Geen, both of Analog Devices, Micromachine Products Division, Cambridge, MA, USA.

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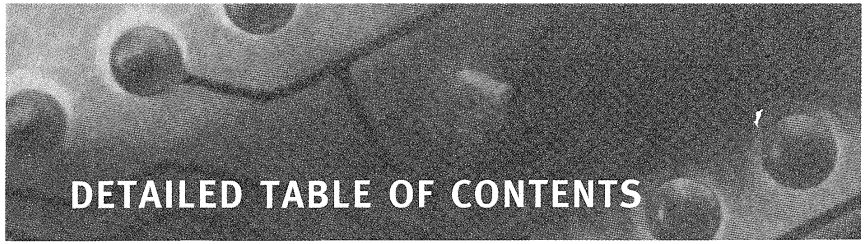

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PREFACE

Microelectronic Circuits, fifth edition, is intended as a text for the core courses in electronic circuits taught to majors in electrical and computer engineering. It should also prove useful to engineers and other professionals wishing to update their knowledge through self-study.

As was the case with the first four editions, the objective of this book is to develop in the reader the ability to analyze and design electronic circuits, both analog and digital, discrete and integrated. While the application of integrated circuits is covered, emphasis is placed on transistor circuit design. This is done because of our belief that even if the majority of those studying the book were not to pursue a career in IC design, knowledge of what is inside the IC package would enable intelligent and innovative application of such chips. Furthermore, with the advances in VLSI technology and design methodology, IC design itself is becoming accessible to an increasing number of engineers.

PREREQUISITES

The prerequisite for studying the material in this book is a first course in circuit analysis. As a review, some linear circuits material is included here in appendixes: specifically, two-port network parameters in Appendix B; some useful network theorems in Appendix C; single-time-constant circuits in Appendix D; and *s*-domain analysis in Appendix E. No prior knowledge of physical electronics is assumed. All required device physics is included, and Appendix A provides a brief description of IC fabrication.

NEW TO THIS EDITION

Although the philosophy and pedagogical approach of the first four editions have been retained, several changes have been made to both organization and coverage.

1. The book has been reorganized into three parts. Part I: Devices and Basic Circuits, composed of the first five chapters, provides a coherent and reasonably comprehensive single-semester introductory course in electronics. Similarly, Part II: Analog and Digital Integrated Circuits (Chapters 6–10) presents a body of material suitable for a second one-semester course. Finally, four carefully chosen subjects are included in Part III: Selected Topics. These can be used as enhancements or substitutions for some of the material in earlier chapters, as resources for projects or thesis work, and/or as part of a third course.
2. Each chapter is organized so that the essential "must-cover" topics are placed first, and the more specialized material appears last. This allows considerable flexibility in teaching and learning from the book.
3. Chapter 4, MOSFETs, and Chapter 5, BJTs, have been completely rewritten, updated, and made completely independent of each other. The MOSFET chapter is placed first to reflect the fact that it is currently the most significant electronics device by a wide margin. However, if desired, the BJT can be covered first. Also, the identical structure of the two chapters makes teaching and learning about the second device easier and faster.

4. To make the first course comprehensive, both Chapters 4 and 5 include material on amplifier and digital-logic circuits. In addition, the frequency response of the basic common-source (common-emitter) amplifier is included. This is important for students who might not take a second course in electronics.
5. A new chapter on integrated-circuit (IC) amplifiers (Chapter 6) is added. It begins with a comprehensive comparison between the MOSFET and the BJT. Typical parameter values of devices produced by modern submicron fabrication processes are given and utilized in the examples, exercises, and end-of-chapter problems. The study of each amplifier configuration includes its frequency response. This should make the study of amplifier frequency response more interesting and somewhat easier.
6. The material on differential and multistage amplifiers in Chapter 7 has been rewritten to present the MOSFET differential pair first. Here also, the examples, exercises, and problems have been expanded and updated to utilize parameter values representative of modern submicron technologies.
7. Throughout the book, greater emphasis is placed on MOSFET circuits.
8. To make room for new material, some of the topics that have become less current, such as JFETs and TTL, or have remained highly specialized, such as GaAs devices and circuits, have been removed from the book. However, they are made available on the CD accompanying the book and on the book's website.
9. As a study aid and for easy reference, many summary tables have been added.
10. The review exercises, examples, and end-of-chapter problems have been updated and their numbers and variety increased.
11. The SPICE sections have been rewritten and the SPICE examples now utilize schematic entry. To enable further experimentation, the files for all SPICE examples are provided on the CD and website.

THE CD-ROM AND THE WEBSITE

A CD-ROM accompanies this book. It contains much useful supplementary information and material intended to enrich the student's learning experience. These include (1) A Student's Edition of OrCAD PSpice 9.2. (2) The input files for all the SPICE examples in this book. (3) A link to the book's website accessing PowerPoint slides of every figure in this book that students can print and carry to class to facilitate taking notes. (4) Bonus text material of specialized topics not covered in the current edition of the textbook. These include: JFETs, GaAs devices and circuits, and TTL circuits.

A website for the book has been set up (www.sedrasmith.org). Its content will change frequently to reflect new developments in the field. It features SPICE models and files for all PSpice examples, links to industrial and academic websites of interest, and a message center to communicate with the authors. There is also a link to the Higher Education Group of Oxford University Press so professors can receive complete text support.

EMPHASIS ON DESIGN

It has been our philosophy that circuit design is best taught by pointing out the various trade-offs available in selecting a circuit configuration and in selecting component values for a given configuration. The emphasis on design has been increased in this edition by including more design examples, exercise problems, and end-of-chapter problems. Those exercises and end-of-chapter problems that are considered "design-oriented" are indicated with a D. Also, the most valuable design aid, SPICE, is utilized throughout the book, as already outlined.

EXERCISES, END-OF-CHAPTER PROBLEMS, AND ADDITIONAL SOLVED PROBLEMS

Over 450 exercises are integrated throughout the text. The answer to each exercise is given below the exercise so students can check their understanding of the material as they read. Solving these exercises should enable the reader to gauge his or her grasp of the preceding material. In addition, more than 1370 end-of-chapter problems, about a third of which are new to this edition, are provided. The problems are keyed to the individual sections and their degree of difficulty is indicated by a rating system: difficult problems are marked with as asterisk (*); more difficult problems with two asterisks (**); and very difficult (and/or time consuming) problems with three asterisks (***). We must admit, however, that this classification is by no means exact. Our rating no doubt had depended to some degree on our thinking (and mood!) at the time a particular problem was created. Answers to about half the problems are given in Appendix H. Complete solutions for all exercises and problems are included in the *Instructor's Manual,* which is available from the publisher for those instructors who adopt the book.

As in the previous four editions, many examples are included. The examples, and indeed most of the problems and exercises, are based on real circuits and anticipate the applications encountered in designing real-life circuits. This edition continues the use of numbered solution steps in the figures for many examples, as an attempt to recreate the dynamics of the classroom.

A recurring request from many of the students who used earlier editions of the book has been for solved problems. To satisfy this need, a book of additional problems with solutions is available with this edition (see the list of available ancillaries later in this preface).

AN OUTLINE FOR THE READER

The book starts with an introduction to the basic concepts of electronics in Chapter 1. Signals, their frequency spectra, and their analog and digital forms are presented. Amplifiers are introduced as circuit building blocks and their various types and models are studied. The basic element of digital electronics, the digital logic inverter, is defined in terms of its voltage-transfer characteristic, and its various implementations using voltage and current switches are discussed. This chapter also establishes some of the terminology and conventions used throughout the text.

The next four chapters are devoted to the study of electronic devices and basic circuits and constitute the bulk of Part I of the text. Chapter 2 deals with operational amplifiers, their terminal characteristics, simple applications, and limitations. We have chosen to discuss the op amp as a circuit building block at this early stage simply because it is easy to deal with and because the student can experiment with op-amp circuits that perform nontrivial tasks with relative ease and with a sense of accomplishment. We have found this approach to be highly motivating to the student. We should point out, however, that part or all of this chapter can be skipped and studied at a later stage (for instance in conjunction with Chapter 7, Chapter 8, and/or Chapter 9) with no loss of continuity.

Chapter 3 is devoted to the study of the most fundamental electronic device, the *pn* junction diode. The diode terminal characteristics and its hierarchy of models and basic circuit

applications are presented. To understand the physical operation of the diode, and indeed of the MOSFET and the BJT, a concise but substantial introduction to semiconductors and the *pn* junction is provided. This material is placed near the end of the chapter (Section 3.7) so that part or all of it can be skipped by those who have already had a course in physical electronics.

Chapters 4 and 5 deal with the two major electronic devices—the MOS field-effect transistor (MOSFET) and the bipolar junction transistor (BJT), respectively. The two chapters have an identical structure and are completely independent of each other and thus, can be covered in either order. Each chapter begins with a study of the device structure and its physical operation, leading to a description of its terminal characteristics. Then, to establish in the reader a high degree of familiarity with the operation of the transistor as a circuit element, a large number of examples are presented of dc circuits utilizing the device. The large-signal operation of the basic common-source (common-emitter) circuit is then studied and used to delineate the region over which the device can be used as a linear amplifier from those regions where it can be used as a switch. This makes clear the need for biasing the transistor and leads naturally to the study of biasing methods. At this point, the biasing methods used are mostly for discrete circuits, leaving the study of IC biasing to Chapter 6. Next, small-signal operation is studied and small-signal models are derived. This is followed by a study of the basic configurations of discrete-circuit amplifiers. The internal capacitive effects that limit the high-frequency operation of the transistor are then studied, and the high-frequency equivalent-circuit model is presented. This model is then used to determine the high-frequency response of a common-source (common-emitter) amplifier. As well, the low-frequency response resulting from the use of coupling and bypass capacitors is also presented. The basic digital-logic inverter circuit is then studied. Both chapters conclude with a study of the transistor models used in SPICE together with circuit-simulation examples using PSpice. This description should indicate that Chapters 4 and 5 contain the essential material for a first course in electronics.

Part II: Analog and Digital Integrated Circuits (Chapters 6–10) begins with a comprehensive compilation and comparison of the properties of the MOSFET and the BJT. The comparison is facilitated by the provision of typical parameter values of devices fabricated with modern process technologies. Following a study of biasing methods employed in IC amplifier design (Section 6.3), and some basic background material for the analysis of high-frequency amplifier response (Section 6.4), the various configurations of single-stage IC amplifiers are presented in a systematic manner. In each case, the MOS circuit is presented first. Some transistor–pair configurations that are usually treated as a single stage, such as the cascode and the Darlington circuits, are also studied. Each section includes a study of the high-frequency response of the particular amplifier configuration. Again, we believe that this "in-situ" study of frequency response is superior to the traditional approach of postponing all coverage of frequency response to a later chapter. As in other chapters, the more specialized material, including advanced current–mirror and current–source concepts, is placed in the second half of the chapter, allowing the reader to skip some of this material in a first reading. This chapter should provide an excellent preparation for an in-depth study of analog IC design.

The study of IC amplifiers is continued in Chapter 7 where the emphasis is on two major topics: differential amplifiers and multistage amplifiers. Here again, the MOSFET differential pair is treated first. Also, frequency response is discussed where needed, including in the two examples of multistage amplifiers.

Chapter 8 deals with the important topic of feedback. Practical circuit applications of negative feedback are presented. We also discuss the stability problem in feedback amplifiers and treat frequency compensation in some detail.

Chapter 9 integrates the material on analog IC design presented in the preceding three chapters and applies it to the analysis and design of two major analog IC functional blocks: op amps and data converters. Both CMOS and bipolar op amps are studied. The data-converter sections provide a bridge to the study of digital CMOS logic circuits in Chapter 10.

Chapter 10 builds on the introduction to CMOS logic circuits in Section 4.10 and includes a carefully selected set of topics on static and dynamic CMOS logic circuits that round out the study of analog and digital ICs in Part II.

The study of digital circuits is continued in the first of the four selected-topics chapters that comprise Part III. Specifically, Chapter 11 deals with memory and related circuits, such as latches, flip-flops, and monostable and stable multivibrators. As well, two somewhat specialized but significant digital circuit technologies are studied: emitter-coupled logic (ECL) and BiCMOS. The two digital chapters (10 and 11) together with the earlier material on digital circuits should prepare the reader well for a subsequent course on digital IC design or VLSI circuits.

The next two chapters of Part III, Chapters 12 and 13, are application or system oriented. Chapter 12 is devoted to the study of analog-filter design and tuned amplifiers. Chapter 13 presents a study of sinusoidal oscillators, waveform generators, and other nonlinear signal-processing circuits.

The last chapter of the book, Chapter 14, deals with various types of amplifier output stages. Thermal design is studied, and examples of IC power amplifiers are presented.

The eight appendixes contain much useful background and supplementary material. We wish to draw the reader's attention in particular to Appendix A, which provides a concise introduction to the important topic of IC fabrication technology including IC layout.

COURSE ORGANIZATION

The book contains sufficient material for a sequence of two single-semester courses (each of 40 to 50 lecture hours). The organization of the book provides considerable flexibility in course design. In the following, we suggest various possibilities for the two courses.

The First Course

The most obvious package for the first course consists of Chapters 1 through 5. However, if time is limited, some or all of the following sections can be postponed to the second course: 1.6, 1.7, 2.6, 2.7, 2.8, 3.6, 3.8, 4.8, 4.9, 4.10, 4.11, 5.8, 5.9, and 5.10. It is also quite possible to omit Chapter 2 altogether from this course. Also, it is possible to concentrate on the MOSFET (Chapter 4) and cover the BJT (Chapter 5) only partially and/or more quickly. Covering Chapter 5 thoroughly and Chapter 4 only partially and/or more quickly is also possible—but not recommended! An entirely analog first course is also possible by omitting Sections 1.7, 4.10, and 5.10. A digitally oriented first course is also possible. It would consist of the following sections; 1.1, 1.2, 1.3, 1.4, 1.7, 1.8, 3.1, 3.2, 3.3, 3.4, 3.7, 4.1, 4.2, 4.3, 4.4, 4.10, 4.12, 5.1, 5.2, 5.3, 5.4, 5.10, 5.11, all of Chapter 10, and selected topics from Chapter 11. Also, if time permits, some material from Chapter 2 on op amps would be beneficial.

The Second Course

An excellent place to begin the second course is Chapter 6 where Section 6.2 can serve as a review of the MOSFET and BJT characteristics. Ideally, the second course would cover

Chapters 6 through 10 (assuming, of course, that the first course covered Chapters 1 through 5). If time is short, either Chapter 10 can postponed to a subsequent course on digital circuits and/or some sections of Chapters 6–9 can be omitted. One possibility would be to de-emphasize bipolar circuits by omitting some or all of the bipolar sections in Chapters 6, 7, and 9. Another would be to reduce somewhat the coverage of feedback (Chapter 8). Also, data converters can be easily deleted from the second course. Still, for Chapter 9, perhaps only CMOS op amps need to be covered and the 741 deleted or postponed. It is also possible to replace some of the material from Chapters 6–10 by selected topics from Chapters 11–14. For instance, in an entirely analog second course, Chapter 10 can be replaced by a selection of topics from Chapters 13–14.

ANCILLARIES

A complete set of ancillary materials is available with this text to support your course.

For the Instructor

The *Instructor's Manual with Transparency Masters* provides complete worked solutions to all the exercises in each chapter and all the end-of-chapter problems in the text. It also contains 200 transparency masters that duplicate the figures in the text most often used in class.

A set of *Transparency Acetates* of the 200 most important figures in the book.

A *PowerPoint CD* with slides of every figure in the book and each corresponding caption.

For the Student and the Instructor

The *CD-ROM* included with every new copy of the textbook contains SPICE input files, a Student Edition of OrCAD PSpice 9.2 Lite Edition, a link to the website featuring PowerPoint slides of the book's illustrations, and bonus topics.

Laboratory Explorations for Microelectronic Circuits, 5th edition, by Kenneth C. Smith (KC), contains laboratory experiments and instructions for the major topics studied in the text.

KC's Problems and Solutions for Microelectronic Circuits, 5th edition, by Kenneth C. Smith (KC), contains hundreds of additional study problems with complete solutions, for students who want more practice.

SPICE, 2nd edition, by Gordon Roberts of McGill University and Adel Sedra, provides a detailed treatment of SPICE and its application in the analysis and design of circuits of the type studied in this book.

ACKNOWLEDGMENTS

Many of the changes in this fifth edition were made in response to feedback received from some of the instructors who adopted the fourth edition. We are grateful to all those who took the time to write to us. In addition, the following reviewers provided detailed commentary on the fourth edition and suggested many of the changes that we have incorporated in this revision. To all of them, we extend our sincere thanks: Maurice Aburdene, Bucknell University; Patrick L. Chapman, University of Illinois at Urbana-Champaign; Artice Davis, San Jose State University; Paul M. Furth, New Mexico State University; Roobik Gharabagi, St. Louis University; Reza Hashemian, Northern Illinois University; Ward J. Helms, University of Washington; Hsiung Hsu, Ohio State University; Marian Kazimierczuk, Wright State University; Roger King, University of Toledo; Robert J. Krueger, University of Wisconsin-Milwaukee; Un-Ku Moon, Oregon State University; John A. Ringo, Washington State University; Zvi S. Roth, Florida Atlantic University; Mulukutla Sarma, Northeastern University; John Scalzo, Louisiana State University; Ali Sheikholeslami, University of Toronto; Pierre Schmidt, Florida International University; Charles Sullivan, Dartmouth College; Gregory M. Wierzba, Michigan State University; and Alex Zaslavsky, Brown University.

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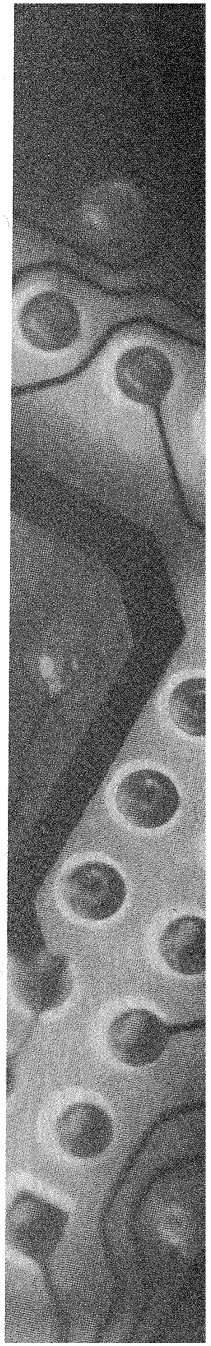
If there is a single person at Oxford University Press that is responsible for this book coming out on time and looking so good, it is our Managing Editor, Karen Shapiro: She has been simply great, and we are deeply indebted to her. We also wish to thank our families for their support and understanding.

Adel S. Sedra
Kenneth C. Smith

MICROELECTRONIC CIRCUITS



PART I

DEVICES AND BASIC CIRCUITS

INTRODUCTION

Part I, *Devices and Basic Circuits,* includes the most fundamental and essential topics for the study of electronic circuits. At the same time, it constitutes a complete package for a first course on the subject.

Besides silicon diodes and transistors, the basic electronic devices, the op amp is studied in Part I. Although not an electronic device in the most fundamental sense, the op amp is commercially available as an integrated circuit (IC) package and has well-defined terminal characteristics. Thus, despite the fact that the op amp's internal circuit is complex, typically incorporating 20 or more transistors, its almost-ideal terminal behavior makes it possible to treat the op amp as a circuit element and to use it in the design of powerful circuits, as we do in Chapter 2, without any knowledge of its internal construction. We should mention, however, that the study of op amps can be delayed to a later point, and Chapter 2 can be skipped with no loss of continuity.

The most basic silicon device is the diode. In addition to learning about diodes and a sample of their applications, Chapter 3 also introduces the general topic of device modeling for the purpose of circuit analysis and design. Also, Section 3.7 provides a substantial introduction to the physical operation of semiconductor devices. This subject is then continued in Section 4.1 for the MOSFET and in Section 5.1 for the BJT. Taken together, these three sections provide a physical background sufficient for the study of electronic circuits at the level presented in this book.

The heart of this book, and of any electronics course, is the study of the two transistor types in use today: the MOS field-effect transistor (MOSFET) in Chapter 4 and the bipolar junction transistor (BJT) in Chapter 5. These two chapters have been written to be completely independent of one another and thus can be studied in either desired order. Furthermore, the two chapters have the same structure, making it easier and faster to study the second device, as well as to draw comparisons between the two device types.

Chapter 1 provides both an introduction to the study of electronics and a number of important concepts for the study of amplifiers (Sections 1.4–1.6) and of digital circuits (Section 1.7).

Each of the five chapters concludes with a section on the use of SPICE simulation in circuit analysis and design. Of particular importance here are the device models employed by SPICE. Finally, note that as in most of the chapters of this book, the *must-know* material is placed near the beginning of a chapter while the *good-to-know* topics are placed in the latter part of the chapter. Some of this latter material can therefore be skipped in a first course and covered at a later time, when needed.

CHAPTER 1

Introduction to Electronics

INTRODUCTION

The subject of this book is modern electronics, a field that has come to be known as **microelectronics. Microelectronics** refers to the integrated-circuit (IC) technology that at the time of this writing is capable of producing circuits that contain millions of components in a small piece of silicon (known as a **silicon chip**) whose area is on the order of 100 mm^2. One such microelectronic circuit, for example, is a complete digital computer, which accordingly is known as a **microcomputer** or, more generally, a **microprocessor.**

In this book we shall study electronic devices that can be used singly (in the design of **discrete circuits**) or as components of an **integrated-circuit (IC)** chip. We shall study the design and analysis of interconnections of these devices, which form discrete and integrated circuits of varying complexity and perform a wide variety of functions. We shall also learn about available IC chips and their application in the design of electronic systems.

The purpose of this first chapter is to introduce some basic concepts and terminology. In particular, we shall learn about signals and about one of the most important signal-processing functions electronic circuits are designed to perform, namely, signal amplification. We shall then look at models for linear amplifiers. These models will be employed in subsequent chapters in the design and analysis of actual amplifier circuits.

Whereas the amplifier is the basic element of analog circuits, the logic inverter plays this role in digital circuits. We shall therefore take a preliminary look at the digital inverter, its circuit function, and important characteristics.

In addition to motivating the study of electronics, this chapter serves as a bridge between the study of linear circuits and that of the subject of this book: the design and analysis of electronic circuits.

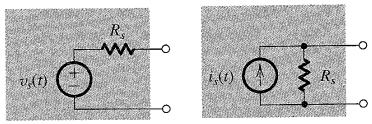
1.1 SIGNALS

Signals contain information about a variety of things and activities in our physical world. Examples abound: Information about the weather is contained in signals that represent the air temperature, pressure, wind speed, etc. The voice of a radio announcer reading the news into a microphone provides an acoustic signal that contains information about world affairs. To monitor the status of a nuclear reactor, instruments are used to measure a multitude of relevant parameters, each instrument producing a signal.

To extract required information from a set of signals, the observer (be it a human or a machine) invariably needs to **process** the signals in some predetermined manner. This **signal processing** is usually most conveniently performed by electronic systems. For this to be possible, however, the signal must first be converted into an electric signal, that is, a voltage or a current. This process is accomplished by devices known as **transducers.** A variety of transducers exist, each suitable for one of the various forms of physical signals. For instance, the sound waves generated by a human can be converted into electric signals using a microphone, which is in effect a pressure transducer. It is not our purpose here to study transducers; rather, we shall assume that the signals of interest already exist in the electrical domain and represent them by one of the two equivalent forms shown in Fig. 1.1. In Fig. 1.1(a) the signal is represented by a voltage source $v_s(t)$ having a source resistance R_s. In the alternate representation of Fig. 1.1(b) the signal is represented by a current source $i_s(t)$ having a source resistance R_s. Although the two representations are equivalent, that in Fig. 1.1(a) (known as the Thévenin form) is preferred when R_s is low. The representation of Fig. 1.1(b) (known as the Norton form) is preferred when R_s is high. The reader will come to appreciate this point later in this chapter when we study the different types of amplifiers. For the time being, it is important to be familiar with Thévenin's and Norton's theorems (for a brief review, see Appendix D) and to note that for the two representations in Fig. 1.1 to be equivalent, their parameters are related by

$$v_s(t) = R_s i_s(t)$$

From the discussion above, it should be apparent that a signal is a time-varying quantity that can be represented by a graph such as that shown in Fig. 1.2. In fact, the information content of the signal is represented by the changes in its magnitude as time progresses; that is, the information is contained in the "wiggles" in the signal waveform. In general, such waveforms are difficult to characterize mathematically. In other words, it is not easy to describe succinctly an arbitrary-looking waveform such as that of Fig. 1.2. Of course, such a



(a) (b)

FIGURE 1.1 Two alternative representations of a signal source: **(a)** the Thévenin form, and **(b)** the Norton form.

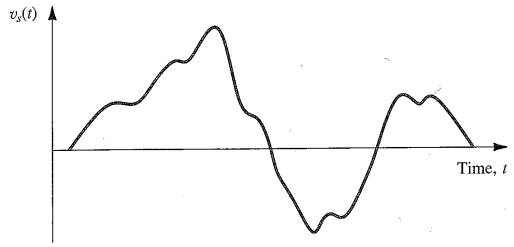


FIGURE 1.2 An arbitrary voltage signal $v_s(t)$.

description is of great importance for the purpose of designing appropriate signal-processing circuits that perform desired functions on the given signal.

EXERCISES

1.1 For the signal-source representations shown in Figs. 1.1(a) and 1.1(b), what are the open-circuit output voltages that would be observed? If, for each, the output terminals are short-circuited (i.e., wired together), what current would flow? For the representations to be equivalent, what must the relationship be between v_s, i_s, and R_s?

Ans. For (a), $v_{oc} = v_s(t)$; for (b), $v_{oc} = R_s i_s(t)$; for (a), $i_{sc} = v_s(t)/R_s$; for (b), $i_{sc} = i_s(t)$; for equivalency, $v_s(t) = R_s i_s(t)$

1.2 A signal source has an open-circuit voltage of 10 mV and a short-circuit current of 10 μA. What is the source resistance?

Ans. 1 kΩ

1.2 FREQUENCY SPECTRUM OF SIGNALS

An extremely useful characterization of a signal, and for that matter of any arbitrary function of time, is in terms of its **frequency spectrum.** Such a description of signals is obtained through the mathematical tools of **Fourier series** and **Fourier transform.**[1] We are not interested at this point in the details of these transformations; suffice it to say that they provide the means for representing a voltage signal $v_s(t)$ or a current signal $i_s(t)$ as the sum of sine-wave signals of different frequencies and amplitudes. This makes the sine wave a very important signal in the analysis, design, and testing of electronic circuits. Therefore, we shall briefly review the properties of the sinusoid.

Figure 1.3 shows a sine-wave voltage signal $v_a(t)$,

$$v_a(t) = V_a \sin \omega t \tag{1.1}$$

[1] The reader who has not yet studied these topics should not be alarmed. No detailed application of this material will be made until Chapter 6. Nevertheless, a general understanding of Section 1.2 should be very helpful when studying early parts of this book.

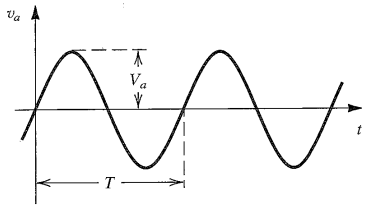


FIGURE 1.3 Sine-wave voltage signal of amplitude V_a and frequency $f = 1/T$ Hz. The angular frequency $\omega = 2\pi f$ rad/s.

where V_a denotes the peak value or amplitude in volts and ω denotes the angular frequency in radians per second; that is, $\omega = 2\pi f$ rad/s, where f is the frequency in hertz, $f = 1/T$ Hz, and T is the period in seconds.

The sine-wave signal is completely characterized by its peak value V_a, its frequency ω, and its phase with respect to an arbitrary reference time. In the case depicted in Fig. 1.3, the time origin has been chosen so that the phase angle is 0. It should be mentioned that it is common to express the amplitude of a sine-wave signal in terms of its root-mean-square (rms) value, which is equal to the peak value divided by $\sqrt{2}$. Thus the rms value of the sinusoid $v_a(t)$ of Fig. 1.3 is $V_a/\sqrt{2}$. For instance, when we speak of the wall power supply in our homes as being 120 V, we mean that it has a sine waveform of $120\sqrt{2}$ volts peak value.

Returning now to the representation of signals as the sum of sinusoids, we note that the Fourier series is utilized to accomplish this task for the special case when the signal is a periodic function of time. On the other hand, the Fourier transform is more general and can be used to obtain the frequency spectrum of a signal whose waveform is an arbitrary function of time.

The Fourier series allows us to express a given periodic function of time as the sum of an infinite number of sinusoids whose frequencies are harmonically related. For instance, the symmetrical square-wave signal in Fig. 1.4 can be expressed as

$$v(t) = \frac{4V}{\pi}(\sin \omega_0 t + \tfrac{1}{3}\sin 3\omega_0 t + \tfrac{1}{5}\sin 5\omega_0 t + \cdots) \tag{1.2}$$

where V is the amplitude of the square wave and $\omega_0 = 2\pi/T$ (T is the period of the square wave) is called the **fundamental frequency.** Note that because the amplitudes of the harmonics progressively decrease, the infinite series can be truncated, with the truncated series providing an approximation to the square waveform.

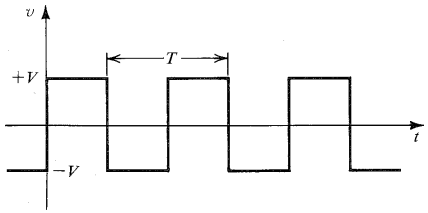


FIGURE 1.4 A symmetrical square-wave signal of amplitude V.

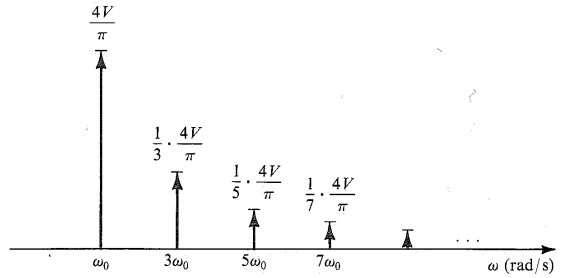


FIGURE 1.5 The frequency spectrum (also known as the line spectrum) of the periodic square wave of Fig. 1.4.

The sinusoidal components in the series of Eq. (1.2) constitute the frequency spectrum of the square-wave signal. Such a spectrum can be graphically represented as in Fig. 1.5, where the horizontal axis represents the angular frequency ω in radians per second.

The Fourier transform can be applied to a nonperiodic function of time, such as that depicted in Fig. 1.2, and provides its frequency spectrum as a continuous function of frequency, as indicated in Fig. 1.6. Unlike the case of periodic signals, where the spectrum consists of discrete frequencies (at ω_0 and its harmonics), the spectrum of a nonperiodic signal contains in general all possible frequencies. Nevertheless, the essential parts of the spectra of practical signals are usually confined to relatively short segments of the frequency (ω) axis—an observation that is very useful in the processing of such signals. For instance, the spectrum of audible sounds such as speech and music extends from about 20 Hz to about 20 kHz—a frequency range known as the **audio band.** Here we should note that although some musical tones have frequencies above 20 kHz, the human ear is incapable of hearing frequencies that are much above 20 kHz. As another example, analog video signals have their spectra in the range of 0 MHz to 4.5 MHz.

We conclude this section by noting that a signal can be represented either by the manner in which its waveform varies with time, as for the voltage signal $v_a(t)$ shown in Fig. 1.2, or in terms of its frequency spectrum, as in Fig. 1.6. The two alternative representations are known as the time-domain representation and the frequency-domain representation, respectively. The frequency-domain representation of $v_a(t)$ will be denoted by the symbol $V_a(\omega)$.

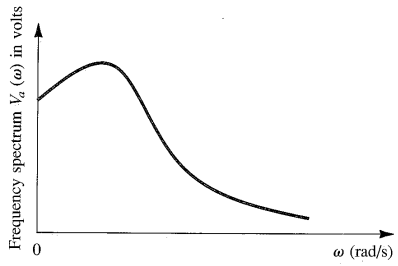


FIGURE 1.6 The frequency spectrum of an arbitrary waveform such as that in Fig. 1.2.

EXERCISES

1.3 Find the frequencies f and ω of a sine-wave signal with a period of 1 ms.

Ans. $f = 1000$ Hz; $\omega = 2\pi \times 10^3$ rad/s

1.4 What is the period T of sine waveforms characterized by frequencies of (a) $f = 60$ Hz? (b) $f = 10^{-3}$ Hz? (c) $f = 1$ MHz?

Ans. 16.7 ms; 1000 s; 1 μs

1.5 The UHF (Ultra High Frequency) television broadcast band begins with channel 14 and extends from 470 MHz to 806 MHz. If 6 MHz is allocated for each channel, how many channels can this band accommodate?

Ans. 56; channels 14 to 69

1.6 When the square-wave signal of Fig. 1.4, whose Fourier series is given in Eq. (1.2), is applied to a resistor, the total power dissipated may be calculated directly using the relationship $P = 1/T \int_0^T (v^2/R)\,dt$ or indirectly by summing the contribution of each of the harmonic components, that is, $P = P_1 + P_3 + P_5 + \cdots$, which may be found directly from rms values. Verify that the two approaches are equivalent. What fraction of the energy of a square wave is in its fundamental? In its first five harmonics? In its first seven? First nine? In what number of harmonics is 90% of the energy? (Note that in counting harmonics, the fundamental at ω_0 is the first, the one at $2\omega_0$ is the second, etc.)

Ans. 0.81; 0.93; 0.95; 0.96; 3

1.3 ANALOG AND DIGITAL SIGNALS

The voltage signal depicted in Fig. 1.2 is called an **analog signal.** The name derives from the fact that such a signal is analogous to the physical signal that it represents. The magnitude of an analog signal can take on any value; that is, the amplitude of an analog signal exhibits a continuous variation over its range of activity. The vast majority of signals in the world around us are analog. Electronic circuits that process such signals are known as **analog circuits.** A variety of analog circuits will be studied in this book.

An alternative form of signal representation is that of a sequence of numbers, each number representing the signal magnitude at an instant of time. The resulting signal is called a **digital signal.** To see how a signal can be represented in this form—that is, how signals can be converted from analog to digital form—consider Fig. 1.7(a). Here the curve represents a voltage signal, identical to that in Fig. 1.2. At equal intervals along the time axis we have marked the time instants t_0, t_1, t_2, and so on. At each of these time instants the magnitude of the signal is measured, a process known as **sampling.** Figure 1.7(b) shows a representation of the signal of Fig. 1.7(a) in terms of its samples. The signal of Fig. 1.7(b) is defined only at the sampling instants; it no longer is a continuous function of time, but rather, it is a **discrete-time signal.** However, since the magnitude of each sample can take any value in a continuous range, the signal in Fig. 1.7(b) is still an analog signal.

Now if we represent the magnitude of each of the signal samples in Fig. 1.7(b) by a number having a finite number of digits, then the signal amplitude will no longer be continuous; rather, it is said to be **quantized, discretized,** or **digitized.** The resulting digital signal then is simply a sequence of numbers that represent the magnitudes of the successive signal samples.

The choice of number system to represent the signal samples affects the type of digital signal produced and has a profound effect on the complexity of the digital circuits required

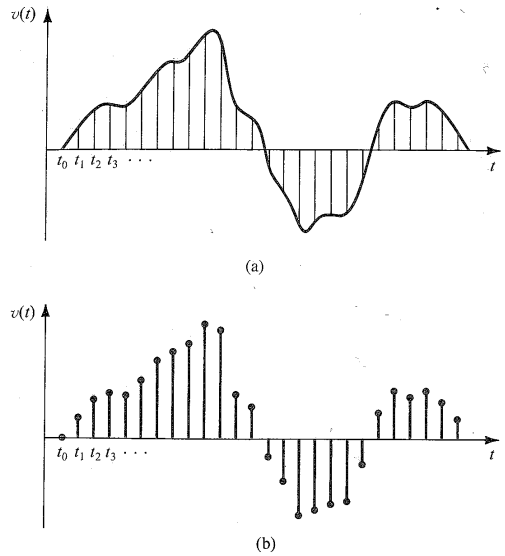


FIGURE 1.7 Sampling the continuous-time analog signal in **(a)** results in the discrete-time signal in **(b).**

to process the signals. It turns out that the **binary** number system results in the simplest possible digital signals and circuits. In a binary system, each digit in the number takes on one of only two possible values, denoted 0 and 1. Correspondingly, the digital signals in binary systems need have only two voltage levels, which can be labeled low and high. As an example, in some of the digital circuits studied in this book, the levels are 0 V and +5 V. Figure 1.8 shows the time variation of such a digital signal. Observe that the waveform is a pulse train with 0 V representing a 0 signal, or logic 0, and +5 V representing logic 1.

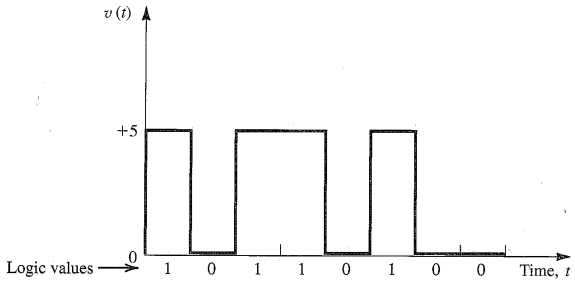


FIGURE 1.8 Variation of a particular binary digital signal with time.

If we use N *b*inary dig*its* (bits) to represent each sample of the analog signal, then the digitized sample value can be expressed as

$$D = b_0 2^0 + b_1 2^1 + b_2 2^2 + \cdots + b_{N-1} 2^{N-1} \tag{1.3}$$

where $b_0, b_1, \ldots, b_{N-1}$, denote the N bits and have values of 0 or 1. Here bit b_0 is the **least significant bit** (LSB), and bit b_{N-1} is the **most significant bit** (MSB). Conventionally, this binary number is written as $b_{N-1}b_{N-2}\ldots b_0$. We observe that such a representation quantizes the analog sample into one of 2^N levels. Obviously the greater the number of bits (i.e., the larger the N), the closer the digital word D approximates the magnitude of the analog sample. That is, increasing the number of bits reduces the *quantization error* and increases the resolution of the analog-to-digital conversion. This improvement is, however, usually obtained at the expense of more complex and hence more costly circuit implementations. It is not our purpose here to delve into this topic any deeper; we merely want the reader to appreciate the nature of analog and digital signals. Nevertheless, it is an opportune time to introduce a very important circuit building block of modern electronic systems: the **analog-to-digital converter** (A/D or ADC) shown in block form in Fig. 1.9. The ADC accepts at its input the samples of an analog signal and provides for each input sample the corresponding N-bit digital representation (according to Eq. 1.3) at its N output terminals. Thus although the voltage at the input might be, say, 6.51 V, at each of the output terminals (say, at the ith terminal), the voltage will be either low (0 V) or high (5 V) if b_i is supposed to be 0 or 1, respectively. We shall study the ADC and its dual circuit the **digital-to-analog converter** (D/A or DAC) in Chapter 9.

Once the signal is in digital form, it can be processed using **digital circuits.** Of course digital circuits can deal also with signals that do not have an analog origin, such as the signals that represent the various instructions of a digital computer.

Since digital circuits deal exclusively with binary signals, their design is simpler than that of analog circuits. Furthermore, digital systems can be designed using a relatively few different kinds of digital circuit blocks. However, a large number (e.g., hundreds of thousands or even millions) of each of these blocks are usually needed. Thus the design of digital circuits poses its own set of challenges to the designer but provides reliable and economic implementations of a great variety of signal processing functions, some of which are not possible with analog circuits. At the present time, more and more of the signal processing functions are being performed digitally. Examples around us abound: from the digital watch and the calculator to digital audio systems and, more recently, digital television. Moreover, some longstanding analog systems such as the telephone communication system are now almost entirely digital. And we should not forget the most important of all digital systems, the digital computer.

The basic building blocks of digital systems are logic circuits and memory circuits. We shall study both in this book, beginning in Section 1.7 with the most fundamental digital circuit, the digital logic inverter.

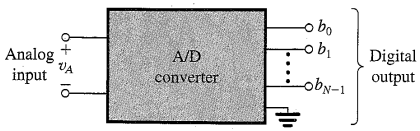


FIGURE 1.9 Block-diagram representation of the analog-to-digital converter (ADC).

One final remark: Although the digital processing of signals is at present all-pervasive, there remain many signal processing functions that are best performed by analog circuits. Indeed, many electronic systems include both analog and digital parts. It follows that a good electronics engineer must be proficient in the design of both analog and digital circuits, or **mixed-signal** or **mixed-mode** design as it is currently known. Such is the aim of this book.

EXERCISE

1.7 Consider a 4-bit digital word $D = b_3b_2b_1b_0$ (see Eq. 1.3) used to represent an analog signal v_A that varies between 0 V and +15 V.
(a) Give D corresponding to v_A = 0 V, 1 V, 2 V, and 15 V.
(b) What change in v_A causes a change from 0 to 1 in: (i) b_0, (ii) b_1, (iii) b_2, and (iv) b_3?
(c) If v_A = 5.2 V, what do you expect D to be? What is the resulting error in representation?
Ans. (a) 0000, 0001, 0010, 1111; (b) +1 V, +2 V, +4 V, +8 V; (c) 0101, −4%

1.4 AMPLIFIERS

In this section, we shall introduce a fundamental signal-processing function that is employed in some form in almost every electronic system, namely, signal amplification. We shall study the amplifier as a circuit building block, that is consider its external characteristics and leave the design of its internal circuit to later chapters.

1.4.1 Signal Amplification

From a conceptual point of view the simplest signal-processing task is that of **signal amplification.** The need for amplification arises because transducers provide signals that are said to be "weak," that is, in the microvolt (μV) or millivolt (mV) range and possessing little energy. Such signals are too small for reliable processing, and processing is much easier if the signal magnitude is made larger. The functional block that accomplishes this task is the **signal amplifier.**

It is appropriate at this point to discuss the need for **linearity** in amplifiers. When amplifying a signal, care must be exercised so that the information contained in the signal is not changed and no new information is introduced. Thus when feeding the signal shown in Fig. 1.2 to an amplifier, we want the output signal of the amplifier to be an exact replica of that at the input, except of course for having larger magnitude. In other words, the "wiggles" in the output waveform must be identical to those in the input waveform. Any change in waveform is considered to be **distortion** and is obviously undesirable.

An amplifier that preserves the details of the signal waveform is characterized by the relationship

$$v_o(t) = A\,v_i(t) \tag{1.4}$$

where v_i and v_o are the input and output signals, respectively, and A is a constant representing the magnitude of amplification, known as **amplifier gain.** Equation (1.4) is a linear relationship; hence the amplifier it describes is a **linear amplifier.** It should be easy to see that if the relationship between v_o and v_i contains higher powers of v_i, then the waveform of v_o will no longer be identical to that of v_i. The amplifier is then said to exhibit **nonlinear distortion.**

The amplifiers discussed so far are primarily intended to operate on very small input signals. Their purpose is to make the signal magnitude larger and therefore are thought of as **voltage amplifiers.** The **preamplifier** in the home stereo system is an example of a voltage amplifier. However, it usually does more than just amplify the signal; specifically, it performs some shaping of the frequency spectrum of the input signal. This topic, however, is beyond our need at this moment.

At this time we wish to mention another type of amplifier, namely, the **power amplifier.** Such an amplifier may provide only a modest amount of voltage gain but substantial current gain. Thus while absorbing little power from the input signal source to which it is connected, often a preamplifier, it delivers large amounts of power to its load. An example is found in the power amplifier of the home stereo system, whose purpose is to provide sufficient power to drive the loudspeaker, which is the amplifier load. Here we should note that the loudspeaker is the output transducer of the stereo system; it converts the electric output signal of the system into an acoustic signal. A further appreciation of the need for linearity can be acquired by reflecting on the power amplifier. A linear power amplifier causes both soft and loud music passages to be reproduced without distortion.

1.4.2 Amplifier Circuit Symbol

The signal amplifier is obviously a two-port network. Its function is conveniently represented by the circuit symbol of Fig. 1.10(a). This symbol clearly distinguishes the input and output ports and indicates the direction of signal flow. Thus, in subsequent diagrams it will not be necessary to label the two ports "input" and "output." For generality we have shown the amplifier to have two input terminals that are distinct from the two output terminals. A more common situation is illustrated in Fig. 1.10(b), where a common terminal exists between the input and output ports of the amplifier. This common terminal is used as a reference point and is called the **circuit ground.**

1.4.3 Voltage Gain

A linear amplifier accepts an input signal $v_I(t)$ and provides at the output, across a load resistance R_L (see Fig. 1.11(a)), an output signal $v_O(t)$ that is a magnified replica of $v_I(t)$. The **voltage gain** of the amplifier is defined by

$$\text{Voltage gain } (A_v) \equiv \frac{v_O}{v_I} \tag{1.5}$$

Fig. 1.11(b) shows the **transfer characteristic** of a linear amplifier. If we apply to the input of this amplifier a sinusoidal voltage of amplitude $\hat{V}$, we obtain at the output a sinusoid of amplitude $A_v\hat{V}$.

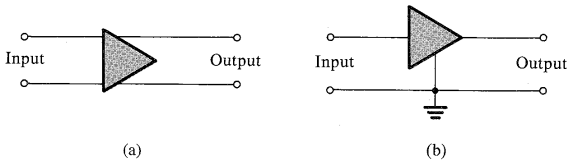


FIGURE 1.10 **(a)** Circuit symbol for amplifier. **(b)** An amplifier with a common terminal (ground) between the input and output ports.

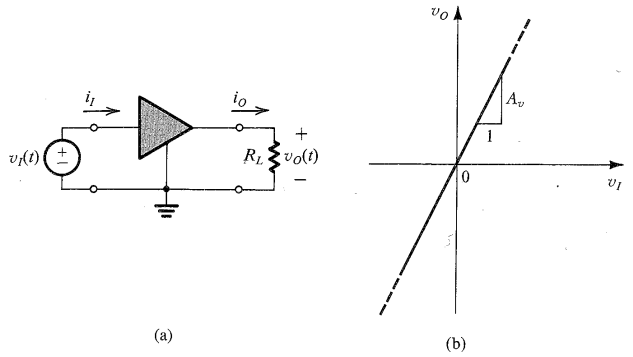


FIGURE 1.11 **(a)** A voltage amplifier fed with a signal $v_I(t)$ and connected to a load resistance R_L. **(b)** Transfer characteristic of a linear voltage amplifier with voltage gain A_v.

1.4.4 Power Gain and Current Gain

An amplifier increases the signal power, an important feature that distinguishes an amplifier from a transformer. In the case of a transformer, although the voltage delivered to the load could be greater than the voltage feeding the input side (the primary), the power delivered to the load (from the secondary side of the transformer) is less than or at most equal to the power supplied by the signal source. On the other hand, an amplifier provides the load with power greater than that obtained from the signal source. That is, amplifiers have power gain. The **power gain** of the amplifier in Fig. 1.11(a) is defined as

$$\text{Power gain } (A_p) \equiv \frac{\text{load power } (P_L)}{\text{input power } (P_I)} \tag{1.6}$$

$$= \frac{v_O i_O}{v_I i_I} \tag{1.7}$$

where i_O is the current that the amplifier delivers to the load (R_L), $i_O = v_O/R_L$, and i_I is the current the amplifier draws from the signal source. The **current gain** of the amplifier is defined as

$$\text{Current gain } (A_i) \equiv \frac{i_O}{i_I} \tag{1.8}$$

From Eqs. (1.5) to (1.8) we note that

$$A_p = A_v A_i \tag{1.9}$$

1.4.5 Expressing Gain in Decibels

The amplifier gains defined above are ratios of similarly dimensioned quantities. Thus they will be expressed either as dimensionless numbers or, for emphasis, as V/V for the voltage gain, A/A for the current gain, and W/W for the power gain. Alternatively, for a number of reasons, some of them historic, electronics engineers express amplifier gain with a logarithmic measure. Specifically the voltage gain A_v can be expressed as

$$\text{Voltage gain in decibels} = 20 \log|A_v| \quad \text{dB}$$

and the current gain A_i can be expressed as

$$\text{Current gain in decibels} = 20 \log|A_i| \quad \text{dB}$$

Since power is related to voltage (or current) squared, the power gain A_p can be expressed in decibels as

$$\text{Power gain in decibels} = 10 \log A_p \quad \text{dB}$$

The absolute values of the voltage and current gains are used because in some cases A_v or A_i may be negative numbers. A negative gain A_v simply means that there is a 180° phase difference between input and output signals; it does not imply that the amplifier is **attenuating** the signal. On the other hand, an amplifier whose voltage gain is, say, –20 dB is in fact attenuating the input signal by a factor of 10 (i.e., $A_v = 0.1$ V/V).

1.4.6 The Amplifier Power Supplies

Since the power delivered to the load is greater than the power drawn from the signal source, the question arises as to the source of this additional power. The answer is found by observing that amplifiers need dc power supplies for their operation. These dc sources supply the extra power delivered to the load as well as any power that might be dissipated in the internal circuit of the amplifier (such power is converted to heat). In Fig. 1.11(a) we have not explicitly shown these dc sources.

Figure 1.12(a) shows an amplifier that requires two dc sources: one positive of value V_1 and one negative of value V_2. The amplifier has two terminals, labeled V^+ and V^-, for connection to the dc supplies. For the amplifier to operate, the terminal labeled V^+ has to be connected to the positive side of a dc source whose voltage is V_1 and whose negative side is connected to the circuit ground. Also, the terminal labeled V^- has to be connected to the negative side of a dc source whose voltage is V_2 and whose positive side is connected to the circuit ground. Now, if the current drawn from the positive supply is denoted I_1 and that from the negative supply is I_2 (see Fig. 1.12(a)), then the dc power delivered to the amplifier is

$$P_{dc} = V_1 I_1 + V_2 I_2$$

If the power dissipated in the amplifier circuit is denoted $P_{\text{dissipated}}$, the power-balance equation for the amplifier can be written as

$$P_{dc} + P_I = P_L + P_{\text{dissipated}}$$

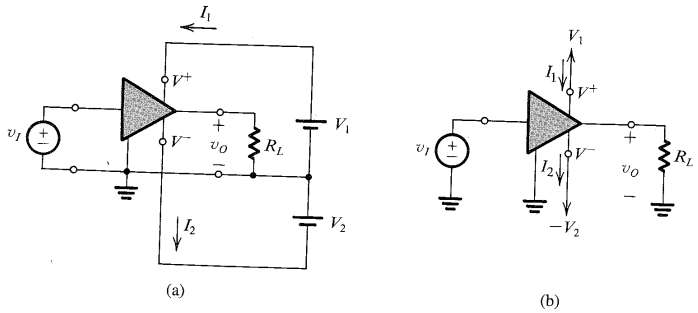


FIGURE 1.12 An amplifier that requires two dc supplies (shown as batteries) for operation.

where P_I is the power drawn from the signal source and P_L is the power delivered to the load. Since the power drawn from the signal source is usually small, the amplifier **efficiency** is defined as

$$\eta \equiv \frac{P_L}{P_{dc}} \times 100 \tag{1.10}$$

The power efficiency is an important performance parameter for amplifiers that handle large amounts of power. Such amplifiers, called power amplifiers, are used, for example, as output amplifiers of stereo systems.

In order to simplify circuit diagrams, we shall adopt the convention illustrated in Fig. 1.12(b). Here the V^+ terminal is shown connected to an arrowhead pointing upward and the V^- terminal to an arrowhead pointing downward. The corresponding voltage is indicated next to each arrowhead. Note that in many cases we will not explicitly show the connections of the amplifier to the dc power sources. Finally, we note that some amplifiers require only one power supply.

EXAMPLE 1.1

Consider an amplifier operating from ±10-V power supplies. It is fed with a sinusoidal voltage having 1 V peak and delivers a sinusoidal voltage output of 9 V peak to a 1-kΩ load. The amplifier draws a current of 9.5 mA from each of its two power supplies. The input current of the amplifier is found to be sinusoidal with 0.1 mA peak. Find the voltage gain, the current gain, the power gain, the power drawn from the dc supplies, the power dissipated in the amplifier, and the amplifier efficiency.

Solution

$$A_v = \frac{9}{1} = 9 \text{ V/V}$$

or

$$A_v = 20 \log 9 \simeq 19.1 \text{ dB}$$

$$\hat{I}_o = \frac{9 \text{ V}}{1 \text{ k}\Omega} = 9 \text{ mA}$$

$$A_i = \frac{\hat{I}_o}{\hat{I}_i} = \frac{9}{0.1} = 90 \text{ A/A}$$

or

$$A_i = 20 \log 90 = 39.1 \text{ dB}$$

$$P_L = V_{o_{\text{rms}}} I_{o_{\text{rms}}} = \frac{9}{\sqrt{2}} \frac{9}{\sqrt{2}} = 40.5 \text{ mW}$$

$$P_I = V_{i_{\text{rms}}} I_{i_{\text{rms}}} = \frac{1}{\sqrt{2}} \frac{0.1}{\sqrt{2}} = 0.05 \text{ mW}$$

$$A_p = \frac{P_L}{P_I} = \frac{40.5}{0.05} = 810 \text{ W/W}$$

or

$$A_p = 10 \log 810 = 29.1 \text{ dB}$$

$$P_{dc} = 10 \times 9.5 + 10 \times 9.5 = 190 \text{ mW}$$

$$P_{dissipated} = P_{dc} + P_I - P_L$$
$$= 190 + 0.05 - 40.5 = 149.6 \text{ mW}$$

$$\eta = \frac{P_L}{P_{dc}} \times 100 = 21.3\%$$

From the above example we observe that the amplifier converts some of the dc power it draws from the power supplies to signal power that it delivers to the load.

1.4.7 Amplifier Saturation

Practically speaking, the amplifier transfer characteristic remains linear over only a limited range of input and output voltages. For an amplifier operated from two power supplies the output voltage cannot exceed a specified positive limit and cannot decrease below a specified negative limit. The resulting transfer characteristic is shown in Fig. 1.13, with the positive and

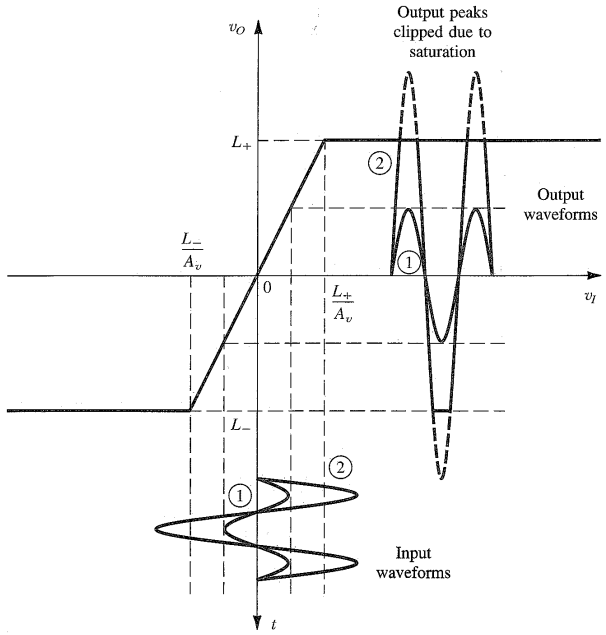


FIGURE 1.13 An amplifier transfer characteristic that is linear except for output saturation.

negative saturation levels denoted L_+ and L_-, respectively. Each of the two saturation levels is usually within a volt or so of the voltage of the corresponding power supply.

Obviously, in order to avoid distorting the output signal waveform, the input signal swing must be kept within the linear range of operation,

$$\frac{L_-}{A_v} \le v_I \le \frac{L_+}{A_v}$$

Figure 1.13 shows two input waveforms and the corresponding output waveforms. We note that the peaks of the larger waveform have been clipped off because of amplifier saturation.

1.4.8 Nonlinear Transfer Characteristics and Biasing

Except for the output saturation effect discussed above, the amplifier transfer characteristics have been assumed to be perfectly linear. In practical amplifiers the transfer characteristic may exhibit nonlinearities of various magnitudes, depending on how elaborate the amplifier circuit is and on how much effort has been expended in the design to ensure linear operation. Consider as an example the transfer characteristic depicted in Fig. 1.14. Such a characteristic is typical of simple amplifiers that are operated from a single (positive) power supply. The transfer characteristic is obviously nonlinear and, because of the single-supply operation, is not centered around the origin. Fortunately, a simple technique exists for obtaining linear amplification from an amplifier with such a nonlinear transfer characteristic.

The technique consists of first **biasing** the circuit to operate at a point near the middle of the transfer characteristic. This is achieved by applying a dc voltage V_b, as indicated in Fig. 1.14, where the operating point is labeled Q and the corresponding dc voltage at the output is V_O. The point Q is known as the **quiescent point,** the **dc bias point,** or simply the **operating point.** The time-varying signal to be amplified, $v_i(t)$, is then superimposed on the dc bias voltage V_I as indicated in Fig. 1.14. Now, as the total instantaneous input $v_I(t)$,

$$v_I(t) = V_I + v_i(t)$$

varies around V_I, the instantaneous operating point moves up and down the transfer curve around the dc operating point Q. In this way, one can determine the waveform of the total instantaneous output voltage $v_O(t)$. It can be seen that by keeping the amplitude of $v_i(t)$ sufficiently small, the instantaneous operating point can be confined to an almost linear segment of the transfer curve centered about Q. This in turn results in the time-varying portion of the output being proportional to $v_i(t)$; that is,

$$v_O(t) = V_O + v_o(t)$$

with

$$v_o(t) = A_v v_i(t)$$

where A_v is the slope of the almost linear segment of the transfer curve; that is,

$$A_v = \left.\frac{dv_O}{dv_I}\right|_{\text{at } Q}$$

In this manner, linear amplification is achieved. Of course, there is a limitation: The input signal must be kept sufficiently small. Increasing the amplitude of the input signal can cause

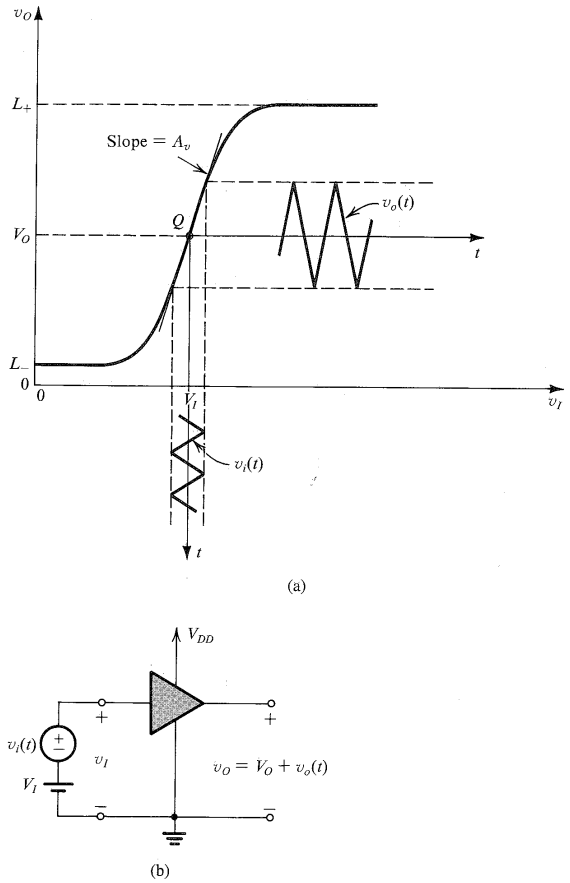


FIGURE 1.14 **(a)** An amplifier transfer characteristic that shows considerable nonlinearity. **(b)** To obtain linear operation the amplifier is biased as shown, and the signal amplitude is kept small. Observe that this amplifier is operated from a single power supply, V_{DD}.

the operation to be no longer restricted to an almost linear segment of the transfer curve. This in turn results in a distorted output signal waveform. Such nonlinear distortion is undesirable: The output signal contains additional spurious information that is not part of the input. We shall use this biasing technique and the associated **small-signal approximation** frequently in the design of transistor amplifiers.

EXAMPLE 1.2

A transistor amplifier has the transfer characteristic

$$v_O = 10 - 10^{-11} e^{40 v_I} \tag{1.11}$$

which applies for $v_I \geq 0$ V and $v_O \geq 0.3$ V. Find the limits L_- and L_+ and the corresponding values of v_I. Also, find the value of the dc bias voltage V_I that results in $V_O = 5$ V and the voltage gain at the corresponding operating point.

Solution

The limit L_- is obviously 0.3 V. The corresponding value of v_I is obtained by substituting $v_O = 0.3$ V in Eq. (1.11); that is,

$$v_I = 0.690 \text{ V}$$

The limit L_+ is determined by $v_I = 0$ and is thus given by

$$L_+ = 10 - 10^{-11} \simeq 10 \text{ V}$$

To bias the device so that $V_O = 5$ V we require a dc input V_I whose value is obtained by substituting $v_O = 5$ V in Eq. (1.11) to find:

$$V_I = 0.673 \text{ V}$$

The gain at the operating point is obtained by evaluating the derivative dv_O/dv_I at $v_I = 0.673$ V. The result is

$$A_v = -200 \text{ V/V}$$

which indicates that this amplifier in an inverting one; that is, the output is 180° out of phase with the input. A sketch of the amplifier transfer characteristic (not to scale) is shown in Fig. 1.15, from which we observe the inverting nature of the amplifier.

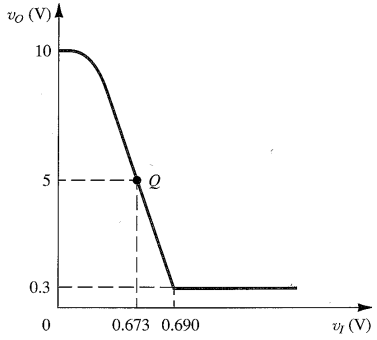


FIGURE 1.15 A sketch of the transfer characteristic of the amplifier of Example 1.2. Note that this amplifier is inverting (i.e., with a gain that is negative).

Once an amplifier is properly biased and the input signal is kept sufficiently small, the operation is assumed to be linear. We can then employ the techniques of linear circuit analysis to analyze the signal operation of the amplifier circuit. This is the topic of Sections 1.5 and 1.6.

1.4.9 Symbol Convention

At this point, we draw the reader's attention to the terminology used above and which we shall employ throughout the book. Total instantaneous quantities are denoted by a lowercase symbol with an uppercase subscript, for example, $i_A(t)$, $v_C(t)$. Direct-current (dc) quantities will be denoted by an uppercase symbol with an uppercase subscript, for example, I_A, V_C. Power-supply (dc) voltages are denoted by an uppercase V with a double-letter uppercase subscript, for example, V_{DD}. A similar notation is used for the dc current drawn from the power supply, for example, I_{DD}. Finally, incremental signal quantities will be denoted by a lowercase symbol with a lowercase subscript, for example, $i_a(t)$, $v_c(t)$. If the signal is a sine wave, then its amplitude is denoted by an uppercase letter with a lowercase subscript, for example, I_a, V_c. This notation is illustrated in Fig. 1.16.

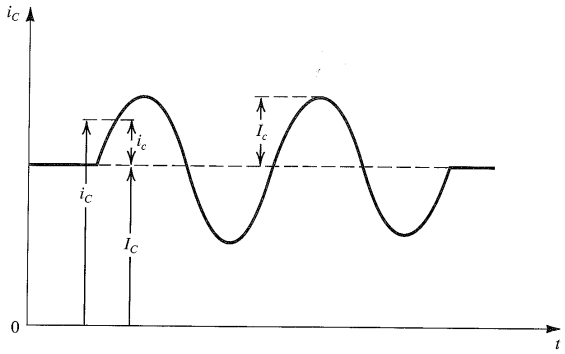


FIGURE 1.16 Symbol convention employed throughout the book.

EXERCISES

1.8 An amplifier has a voltage gain of 100 V/V and a current gain of 1000 A/A. Express the voltage and current gains in decibels and find the power gain.

Ans. 40 dB; 60 dB; 50 dB

1.9 An amplifier operating from a single 15-V supply provides a 12-V peak-to-peak sine-wave signal to a 1-kΩ load and draws negligible input current from the signal source. The dc current drawn from the 15-V supply is 8 mA. What is the power dissipated in the amplifier, and what is the amplifier efficiency?

Ans. 102 mW; 15%

1.10 The objective of this exercise is to investigate the limitation of the small-signal approximation. Consider the amplifier of Example 1.2 with a positive input signal of 1 mV superimposed on the dc bias voltage V_I. Find the corresponding signal at the output for two situations: (a) Assume the amplifier is linear around the operating point; that is, use the value of gain evaluated in Example 1.2. (b) Use the transfer characteristic of the amplifier. Repeat for input signals of 5 mV and 10 mV.

Ans. −0.2 V, −0.204 V; −1 V, −1.107 V; −2 V, −2.459 V

1.5 CIRCUIT MODELS FOR AMPLIFIERS

A good part of this book is concerned with the design of amplifier circuits using transistors of various types. Such circuits will vary in complexity from those using a single transistor to those with 20 or more devices. In order to be able to apply the resulting amplifier circuit as a building block in a system, one must be able to characterize, or **model,** its terminal behavior. In this section, we study simple but effective amplifier models. These models apply irrespective of the complexity of the internal circuit of the amplifier. The values of the model parameters can be found either by analyzing the amplifier circuit or by performing measurements at the amplifier terminals.

1.5.1 Voltage Amplifiers

Figure 1.17(a) shows a circuit model for the voltage amplifier. The model consists of a voltage-controlled voltage source having a gain factor A_{vo}, an input resistance R_i that accounts for the fact that the amplifier draws an input current from the signal source, and an output resistance R_o that accounts for the change in output voltage as the amplifier is called upon to

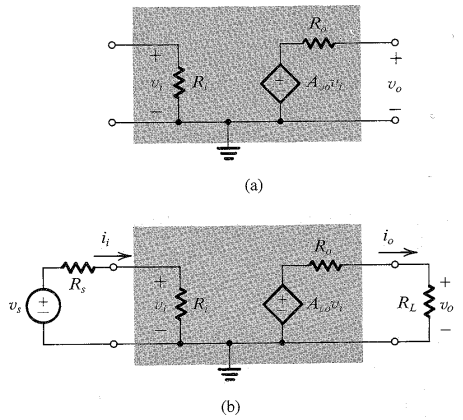


FIGURE 1.17 **(a)** Circuit model for the voltage amplifier. **(b)** The voltage amplifier with input signal source and load.

supply output current to a load. To be specific, we show in Fig. 1.17(b) the amplifier model fed with a signal voltage source v_s having a resistance R_s and connected at the output to a load resistance R_L. The nonzero output resistance R_o causes only a fraction of $A_{vo}v_i$ to appear across the output. Using the voltage-divider rule we obtain

$$v_o = A_{vo}v_i\frac{R_L}{R_L + R_o}$$

Thus the voltage gain is given by

$$A_v \equiv \frac{v_o}{v_i} = A_{vo}\frac{R_L}{R_L + R_o} \tag{1.12}$$

It follows that in order not to lose gain in coupling the amplifier output to a load, the output resistance R_o should be much smaller than the load resistance R_L. In other words, for a given R_L one must design the amplifier so that its R_o is much smaller than R_L. Furthermore, there are applications in which R_L is known to vary over a certain range. In order to keep the output voltage v_o as constant as possible, the amplifier is designed with R_o much smaller than the lowest value of R_L. An ideal voltage amplifier is one with $R_o = 0$. Equation (1.12) indicates also that for $R_L = \infty$, $A_v = A_{vo}$. Thus A_{vo} is the voltage gain of the unloaded amplifier, or the **open-circuit voltage gain.** It should also be clear that in specifying the voltage gain of an amplifier, one must also specify the value of load resistance at which this gain is measured or calculated. If a load resistance is not specified, it is normally assumed that the given voltage gain is the open-circuit gain A_{vo}.

The finite input resistance R_i introduces another voltage-divider action at the input, with the result that only a fraction of the source signal v_s actually reaches the input terminals of the amplifier; that is,

$$v_i = v_s\frac{R_i}{R_i + R_s} \tag{1.13}$$

It follows that in order not to lose a significant portion of the input signal in coupling the signal source to the amplifier input, the amplifier must be designed to have an input resistance R_i much greater than the resistance of the signal source, $R_i \gg R_s$. Furthermore, there are applications in which the source resistance is known to vary over a certain range. To minimize the effect of this variation on the value of the signal that appears at the input of the amplifier, the design ensures that R_i is much greater than the largest value of R_s. An ideal voltage amplifier is one with $R_i = \infty$. In this ideal case both the current gain and power gain become infinite.

The overall voltage gain (v_o/v_s) can be found by combining Eqs. (1.12) and (1.13),

$$\frac{v_o}{v_s} = A_{vo}\frac{R_i}{R_i + R_s}\frac{R_L}{R_L + R_o}$$

There are situations in which one is interested not in voltage gain but only in a significant power gain. For instance, the source signal can have a respectable voltage but a source resistance which is much greater than the load resistance. Connecting the source directly to the load would result in significant signal attenuation. In such a case, one requires an amplifier with a high input resistance (much greater than the source resistance) and a low output resistance (much smaller than the load resistance) but with a modest voltage gain (or even unity gain). Such an amplifier is referred to as a **buffer amplifier.** We shall encounter buffer amplifiers often throughout this book.

EXERCISES

1.11 A transducer characterized by a voltage of 1 V rms and a resistance of 1 MΩ is available to drive a 10-Ω load. If connected directly, what voltage and power levels result at the load? If a unity-gain (i.e., $A_{vo} = 1$) buffer amplifier with 1-MΩ input resistance and 10-Ω output resistance is interposed between source and load, what do the output voltage and power levels become? For the new arrangement find the voltage gain from source to load, and the power gain (both expressed in decibels).

Ans. 10 μV rms; 10^{-11} W; 0.25 V; 6.25 mW; −12 dB; 44 dB

1.12 The output voltage of a voltage amplifier has been found to decrease by 20% when a load resistance of 1 kΩ is connected. What is the value of the amplifier output resistance?

Ans. 250 Ω

1.13 An amplifier with a voltage gain of +40 dB, an input resistance of 10 kΩ, and an output resistance of 1 kΩ is used to drive a 1-kΩ load. What is the value of A_{vo}? Find the value of power gain in dB.

Ans. 100 V/V; 44 dB

1.5.2 Cascaded Amplifiers

To meet given amplifier specifications the need often arises to design the amplifier as a cascade of two or more stages. The stages are usually not identical; rather, each is designed to serve a specific purpose. For instance, the first stage is usually required to have a large input resistance, and the final stage in the cascade is usually designed to have a low output resistance. To illustrate the analysis and design of cascaded amplifiers, we consider a practical example.

EXAMPLE 1.3

Figure 1.18 depicts an amplifier composed of a cascade of three stages. The amplifier is fed by a signal source with a source resistance of 100 kΩ and delivers its output into a load resistance of 100 Ω. The first stage has a relatively high input resistance and a modest gain factor of 10. The second stage has a higher gain factor but lower input resistance. Finally, the last, or output, stage has unity gain but a low output resistance. We wish to evaluate the overall voltage gain, that is, v_L/v_s, the current gain, and the power gain.

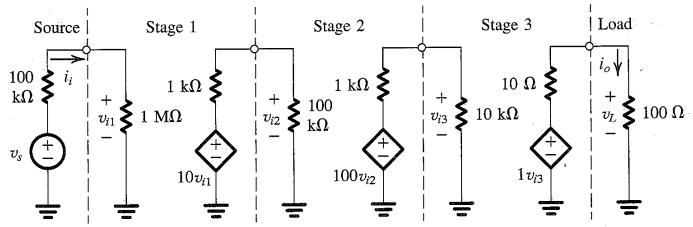


FIGURE 1.18 Three-stage amplifier for Example 1.3.

Solution

The fraction of source signal appearing at the input terminals of the amplifier is obtained using the voltage-divider rule at the input, as follows:

$$\frac{v_{i1}}{v_s} = \frac{1\ \text{M}\Omega}{1\ \text{M}\Omega + 100\ \text{k}\Omega} = 0.909\ \text{V/V}$$

The voltage gain of the first stage is obtained by considering the input resistance of the second stage to be the load of the first stage; that is,

$$A_{v1} \equiv \frac{v_{i2}}{v_{i1}} = 10\frac{100\ \text{k}\Omega}{100\ \text{k}\Omega + 1\ \text{k}\Omega} = 9.9\ \text{V/V}$$

Similarly, the voltage gain of the second stage is obtained by considering the input resistance of the third stage to be the load of the second stage,

$$A_{v2} \equiv \frac{v_{i3}}{v_{i2}} = 100\frac{10\ \text{k}\Omega}{10\ \text{k}\Omega + 1\ \text{k}\Omega} = 90.9\ \text{V/V}$$

Finally, the voltage gain of the output stage is as follows:

$$A_{v3} \equiv \frac{v_L}{v_{i3}} = 1\frac{100\ \Omega}{100\ \Omega + 10\ \Omega} = 0.909\ \text{V/V}$$

The total gain of the three stages in cascade can be now found from

$$A_v \equiv \frac{v_L}{v_{i1}} = A_{v1}A_{v2}A_{v3} = 818\ \text{V/V}$$

or 58.3 dB.

To find the voltage gain from source to load, we multiply A_v by the factor representing the loss of gain at the input; that is,

$$\frac{v_L}{v_s} = \frac{v_L}{v_{i1}}\frac{v_{i1}}{v_s} = A_v\frac{v_{i1}}{v_s}$$
$$= 818 \times 0.909 = 743.6\ \text{V/V}$$

or 57.4 dB.

The current gain is found as follows:

$$A_i \equiv \frac{i_o}{i_i} = \frac{v_L/100\ \Omega}{v_{i1}/1\ \text{M}\Omega}$$
$$= 10^4 \times A_v = 8.18 \times 10^6\ \text{A/A}$$

or 138.3 dB.

The power gain is found from

$$A_p \equiv \frac{P_L}{P_I} = \frac{v_L i_o}{v_{i1} i_i}$$
$$= A_v A_i = 818 \times 8.18 \times 10^6 = 66.9 \times 10^8\ \text{W/W}$$

or 98.3 dB. Note that

$$A_p(\text{dB}) = \tfrac{1}{2}[A_v(\text{dB}) + A_i(\text{dB})]$$

A few comments on the cascade amplifier in the above example are in order. To avoid losing signal strength at the amplifier input where the signal is usually very small, the first stage is designed to have a relatively large input resistance (1 MΩ), which is much larger than the source resistance. The trade-off appears to be a moderate voltage gain (10 V/V). The second stage does not need to have such a high input resistance; rather, here we need to realize the bulk of the required voltage gain. The third and final, or output, stage is not asked to provide any voltage gain; rather, it functions as a buffer amplifier, providing a relatively large input resistance and a low output resistance, much lower than R_L. It is this stage that enables connecting the amplifier to the 10-Ω load. These points can be made more concrete by solving the following exercises.

EXERCISES

1.14 What would the overall voltage gain of the cascade amplifier in Example 1.3 be without stage 3?

Ans. 81.8 V/V

1.15 For the cascade amplifier of Example 1.3, let v_s be 1 mV. Find v_{i1}, v_{i2}, v_{i3}, and v_L.

Ans. 0.91 mV; 9 mV; 818 mV; 744 mV

1.16 (a) Model the three-stage amplifier of Example 1.3 (without the source and load) using the voltage amplifier model. What are the values of R_i, A_{vo}, and R_o?

(b) If R_L varies in the range 10 Ω to 1000 Ω, find the corresponding range of the overall voltage gain, v_o/v_s.

Ans. 1 MΩ, 900 V/V, 10 Ω; 409 V/V to 810 V/V

1.5.3 Other Amplifier Types

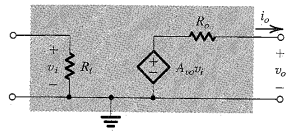
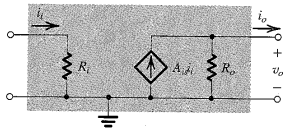
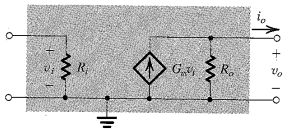
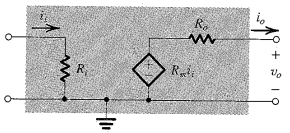
In the design of an electronic system, the signal of interest—whether at the system input, at an intermediate stage, or at the output—can be either a voltage or a current. For instance, some transducers have very high output resistances and can be more appropriately modeled as current sources. Similarly, there are applications in which the output current rather than the voltage is of interest. Thus, although it is the most popular, the voltage amplifier considered above is just one of four possible amplifier types. The other three are the current amplifier, the transconductance amplifier, and the transresistance amplifier. Table 1.1 shows the four amplifier types, their circuit models, the definition of their gain parameters, and the ideal values of their input and output resistances.

1.5.4 Relationships Between the Four Amplifier Models

Although for a given amplifier a particular one of the four models in Table 1.1 is most preferable, *any of the four can be used to model the amplifier.* In fact, simple relationships can be derived to relate the parameters of the various models. For instance, the open-circuit voltage gain A_{vo} can be related to the short-circuit current gain A_{is} as follows: The open-circuit output voltage given by the voltage amplifier model of Table 1.1 is $A_{vo}v_i$. The current amplifier model in the same table gives an open-circuit output voltage of $A_{is}i_iR_o$. Equating these two values and noting that $i_i = v_i/R_i$ gives

$$A_{vo} = A_{is}\left(\frac{R_o}{R_i}\right) \tag{1.14}$$

TABLE 1.1 The Four Amplifier Types

Type	Circuit Model	Gain Parameter	Ideal Characteristics
Voltage Amplifier		Open-Circuit Voltage Gain $A_{vo} \equiv \left.\frac{v_o}{v_i}\right\|_{i_o=0}$ (V/V)	$R_i = \infty$ $R_o = 0$
Current Amplifier		Short-Circuit Current Gain $A_{is} \equiv \left.\frac{i_o}{i_i}\right\|_{v_o=0}$ (A/A)	$R_i = 0$ $R_o = \infty$
Transconductance Amplifier		Short-Circuit Transconductance $G_m \equiv \left.\frac{i_o}{v_i}\right\|_{v_o=0}$ (A/V)	$R_i = \infty$ $R_o = \infty$
Transresistance Amplifier		Open-Circuit Transresistance $R_m \equiv \left.\frac{v_o}{i_i}\right\|_{i_o=0}$ (V/A)	$R_i = 0$ $R_o = 0$

Similarly, we can show that

$$A_{vo} = G_m R_o \tag{1.15}$$

and

$$A_{vo} = \frac{R_m}{R_i} \tag{1.16}$$

The expressions in Eqs. (1.14) to (1.16) can be used to relate any two of the gain parameters A_{vo}, A_{is}, G_m, and R_m.

From the amplifier circuit models given in Table 1.1, we observe that the input resistance R_i of the amplifier can be determined by applying an input voltage v_i and measuring (or calculating) the input current i_i; that is, $R_i = v_i/i_i$. The output resistance is found as the ratio of the open-circuit output voltage to the short-circuit output current. Alternatively, the output resistance can be found by eliminating the input signal source (then i_i and v_i will both be zero) and applying a voltage signal v_x to the output of the amplifier. If we denote the current drawn from v_x *into* the output terminals as i_x (note that i_x is opposite in direction to i_o), then $R_o = v_x/i_x$. Although these techniques are conceptually correct, in actual practice more refined methods are employed in measuring R_i and R_o.

The amplifier models considered above are **unilateral;** that is, signal flow is unidirectional, from input to output. Most real amplifiers show some reverse transmission, which is usually undesirable but must nonetheless be modeled. We shall not pursue this point further at this time except to mention that more complete models for linear two-port networks are given in Appendix B. Also, in Chapters 4 and 5, we will augment the models of Table 1.1 to take into account the nonunilateral nature of some transistor amplifiers.

EXAMPLE 1.4

The **bipolar junction transistor (BJT),** which will be studied in Chapter 5, is a three-terminal device that when dc biased and operated with small signals can be modeled by the linear circuit shown in Fig. 1.19(a). The three terminals are the **base (B),** the **emitter (E),** and the **collector (C).** The heart of the model is a transconductance amplifier represented by an input resistance between B and E (denoted r_π), a short-circuit transconductance g_m, and an output resistance r_o.

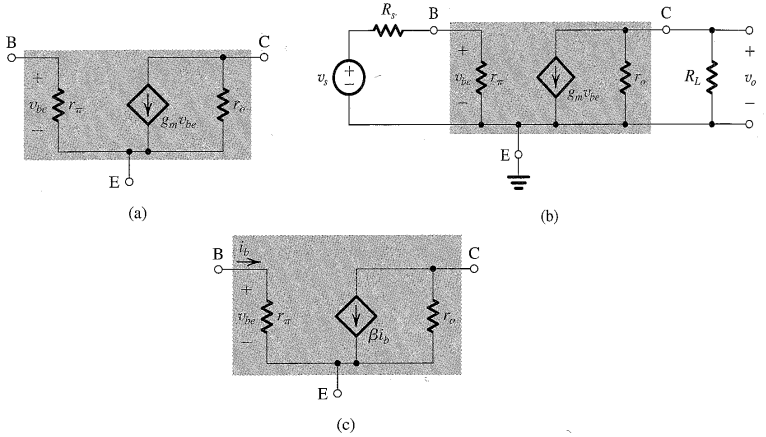


FIGURE 1.19 **(a)** Small-signal circuit model for a bipolar junction transistor (BJT). **(b)** The BJT connected as an amplifier with the emitter as a common terminal between input and output (called a common-emitter amplifier). **(c)** An alternative small-signal circuit model for the BJT.

(a) With the emitter used as a common terminal between input and output, Fig. 1.19(b) shows a transistor amplifier known as a **common-emitter** or **grounded-emitter** circuit. Derive an expression for the voltage gain v_o/v_s, and evaluate its magnitude for the case $R_s = 5$ kΩ, $r_\pi = 2.5$ kΩ, $g_m = 40$ mA/V, $r_o = 100$ kΩ, and $R_L = 5$ kΩ. What would the gain value be if the effect of r_o were neglected?

(b) An alternative model for the transistor in which a current amplifier rather than a transconductance amplifier is utilized is shown in Fig. 1.19(c). What must the short-circuit current-gain β be? Give both an expression and a value.

Solution

(a) Using the voltage-divider rule, we determine the fraction of input signal that appears at the amplifier input as

$$v_{be} = v_s \frac{r_\pi}{r_\pi + R_s} \tag{1.17}$$

Next we determine the output voltage v_o by multiplying the current ($g_m v_{be}$) by the resistance ($R_L \parallel r_o$),

$$v_o = -g_m v_{be}(R_L \parallel r_o) \tag{1.18}$$

Substituting for v_{be} from Eq. (1.17) yields the voltage-gain expression

$$\frac{v_o}{v_s} = -\frac{r_\pi}{r_\pi + R_s} g_m (R_L \parallel r_o) \tag{1.19}$$

Observe that the gain is negative, indicating that this amplifier is inverting. For the given component values,

$$\frac{v_o}{v_s} = -\frac{2.5}{2.5+5} \times 40 \times (5 \parallel 100)$$

$$= -63.5 \text{ V/V}$$

Neglecting the effect of r_o, we obtain

$$\frac{v_o}{v_s} \simeq -\frac{2.5}{2.5+5} \times 40 \times 5$$

$$= -66.7 \text{ V/V}$$

which is quite close to the value obtained including r_o. This is not surprising since $r_o \gg R_L$.

(b) For the model in Fig. 1.19(c) to be equivalent to that in Fig. 1.19(a),

$$\beta i_b = g_m v_{be}$$

But $i_b = v_{be}/r_\pi$; thus,

$$\beta = g_m r_\pi$$

For the values given,

$$\beta = 40 \text{ mA/V} \times 2.5 \text{ k}\Omega$$

$$= 100 \text{ A/A}$$

EXERCISES

1.17 Consider a current amplifier having the model shown in the second row of Table 1.1. Let the amplifier be fed with a signal current-source i_s having a resistance R_s, and let the output be connected to a load resistance R_L. Show that the overall current gain is given by

$$\frac{i_o}{i_s} = A_{is}\frac{R_s}{R_s + R_i}\frac{R_o}{R_o + R_L}$$

1.18 Consider the transconductance amplifier whose model is shown in the third row of Table 1.1. Let a voltage signal-source v_s with a source resistance R_s be connected to the input and a load resistance R_L be connected to the output. Show that the overall voltage-gain is given by

$$\frac{v_o}{v_s} = G_m\frac{R_i}{R_i + R_s}(R_o \parallel R_L)$$

1.19 Consider a transresistance amplifier having the model shown in the third row of Table 1.1. Let the amplifier be fed with a signal current-source i_s having a resistance R_s, and let the output be connected to a load resistance R_L. Show that the overall gain is given by

$$\frac{v_o}{i_s} = R_m\frac{R_s}{R_s + R_i}\frac{R_L}{R_L + R_o}$$

1.20 Find the input resistance between terminals B and G in the circuit shown in Fig. E1.20. The voltage v_x is a test voltage with the input resistance R_{in} defined as $R_{in} = v_x/i_x$.

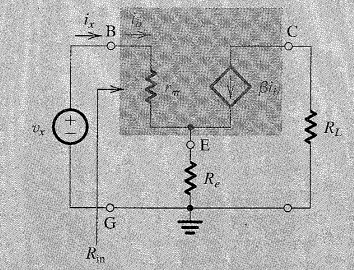


FIGURE E1.20

Ans. $R_{in} = r_\pi + (\beta + 1)R_e$

1.6 FREQUENCY RESPONSE OF AMPLIFIERS

From Section 1.2 we know that the input signal to an amplifier can always be expressed as the sum of sinusoidal signals. It follows that an important characterization of an amplifier is in terms of its response to input sinusoids of different frequencies. Such a characterization of amplifier performance is known as the amplifier frequency response.

1.6.1 Measuring the Amplifier Frequency Response

We shall introduce the subject of amplifier frequency response by showing how it can be measured. Figure 1.20 depicts a linear voltage amplifier fed at its input with a sine-wave signal of amplitude V_i and frequency ω. As the figure indicates, the signal measured at the

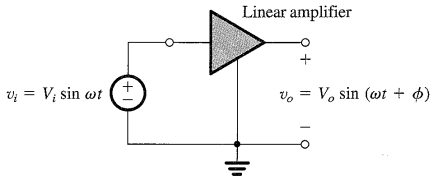


FIGURE 1.20 Measuring the frequency response of a linear amplifier. At the test frequency ω, the amplifier gain is characterized by its magnitude (V_o/V_i) and phase ϕ.

amplifier output also is sinusoidal with exactly the same frequency ω. This is an important point to note: *Whenever a sine-wave signal is applied to a linear circuit, the resulting output is sinusoidal with the same frequency as the input.* In fact, the sine wave is the only signal that does not change shape as it passes through a linear circuit. Observe, however, that the output sinusoid will in general have a different amplitude and will be shifted in phase relative to the input. The ratio of the amplitude of the output sinusoid (V_o) to the amplitude of the input sinusoid (V_i) is the magnitude of the amplifier gain (or transmission) at the test frequency ω. Also, the angle ϕ is the phase of the amplifier transmission at the test frequency ω. If we denote the **amplifier transmission,** or **transfer function** as it is more commonly known, by $T(\omega)$, then

$$|T(\omega)| = \frac{V_o}{V_i}$$
$$\angle T(\omega) = \phi$$

The response of the amplifier to a sinusoid of frequency ω is completely described by $|T(\omega)|$ and $\angle T(\omega)$. Now, to obtain the complete frequency response of the amplifier we simply change the frequency of the input sinusoid and measure the new value for $|T|$ and $\angle T$. The end result will be a table and/or graph of gain magnitude $[|T(\omega)|]$ versus frequency and a table and/or graph of phase angle $[\angle T(\omega)]$ versus frequency. These two plots together constitute the frequency response of the amplifier; the first is known as the **magnitude** or **amplitude response,** and the second is the **phase response.** Finally, we should mention that it is a common practice to express the magnitude of transmission in decibels and thus plot 20 log $|T(\omega)|$ versus frequency.

1.6.2 Amplifier Bandwidth

Figure 1.21 shows the magnitude response of an amplifier. It indicates that the gain is almost constant over a wide frequency range, roughly between ω_1 and ω_2. Signals whose frequencies are below ω_1 or above ω_2 will experience lower gain, with the gain decreasing as we move farther away from ω_1 and ω_2. The band of frequencies over which the gain of the amplifier is almost constant, to within a certain number of decibels (usually 3 dB), is called the **amplifier bandwidth.** Normally the amplifier is designed so that its bandwidth coincides with the spectrum of the signals it is required to amplify. If this were not the case, the amplifier would *distort* the frequency spectrum of the input signal, with different components of the input signal being amplified by different amounts.

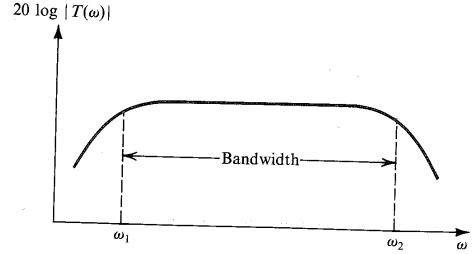


FIGURE 1.21 Typical magnitude response of an amplifier. $|T(\omega)|$ is the magnitude of the amplifier transfer function—that is, the ratio of the output $V_o(\omega)$ to the input $V_i(\omega)$.

1.6.3 Evaluating the Frequency Response of Amplifiers

Above, we described the method used to measure the frequency response of an amplifier. We now briefly discuss the method for analytically obtaining an expression for the frequency response. What we are about to say is just a preview of this important subject, whose detailed study starts in Chapter 4.

To evaluate the frequency response of an amplifier one has to analyze the amplifier equivalent circuit model, taking into account all reactive components.[2] Circuit analysis proceeds in the usual fashion but with inductances and capacitances represented by their reactances. An inductance L has a reactance or impedance $j\omega L$, and a capacitance C has a reactance or impedance $1/j\omega C$ or, equivalently, a susceptance or admittance $j\omega C$. Thus in a *frequency-domain* analysis we deal with impedances and/or admittances. The result of the analysis is the amplifier transfer function $T(\omega)$:

$$T(\omega) = \frac{V_o(\omega)}{V_i(\omega)}$$

where $V_i(\omega)$ and $V_o(\omega)$ denote the input and output signals, respectively. $T(\omega)$ is generally a complex function whose magnitude $|T(\omega)|$ gives the magnitude of transmission or the magnitude response of the amplifier. The phase of $T(\omega)$ gives the phase response of the amplifier.

In the analysis of a circuit to determine its frequency response, the algebraic manipulations can be considerably simplified by using the **complex frequency variable** s. In terms of s, the impedance of an inductance L is sL and that of a capacitance C is $1/sC$. Replacing the reactive elements with their impedances and performing standard circuit analysis, we obtain the transfer function $T(s)$ as

$$T(s) \equiv \frac{V_o(s)}{V_i(s)}$$

Subsequently, we replace s by $j\omega$ to determine the transfer function for **physical frequencies,** $T(j\omega)$. Note that $T(j\omega)$ is the same function we called $T(\omega)$ above;[3] the additional j is included in order to emphasize that $T(j\omega)$ is obtained from $T(s)$ by replacing s with $j\omega$.

1.6.4 Single-Time-Constant Networks

In analyzing amplifier circuits to determine their frequency response, one is greatly aided by knowledge of the frequency response characteristics of single-time-constant (STC) networks. An STC network is one that is composed of, or can be reduced to, one reactive component (inductance or capacitance) and one resistance. Examples are shown in Fig. 1.22. An STC network formed of an inductance L and a resistance R has a time constant $\tau = L/R$. The time constant τ of an STC network composed of a capacitance C and a resistance R is given by $\tau = CR$.

Appendix D presents a study of STC networks and their responses to sinusoidal, step, and pulse inputs. Knowledge of this material will be needed at various points throughout this book, and the reader will be encouraged to refer to the Appendix. At this point we need in particular the frequency response results; we will, in fact, briefly discuss this important topic, now.

---

[2] Note that in the models considered in previous sections no reactive components were included. These were simplified models and cannot be used alone to predict the amplifier frequency response.

[3] At this stage, we are using s simply as a shorthand for $j\omega$. We shall not require detailed knowledge of s-plane concepts until Chapter 6. A brief review of s-plane analysis is presented in Appendix E.

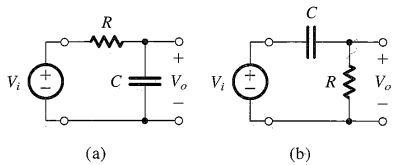


FIGURE 1.22 Two examples of STC networks: **(a)** a low-pass network and **(b)** a high-pass network.

TABLE 1.2 Frequency Response of STC Networks

	Low-Pass (LP)	High-Pass (HP)
Transfer Function $T(s)$	$\frac{K}{1+(s/\omega_0)}$	$\frac{Ks}{s+\omega_0}$
Transfer Function (for physical frequencies) $T(j\omega)$	$\frac{K}{1+j(\omega/\omega_0)}$	$\frac{K}{1-j(\omega_0/\omega)}$
Magnitude Response $\lvert T(j\omega)\rvert$	$\frac{\lvert K\rvert}{\sqrt{1+(\omega/\omega_0)^2}}$	$\frac{\lvert K\rvert}{\sqrt{1+(\omega_0/\omega)^2}}$
Phase Response $\angle T(j\omega)$	$-\tan^{-1}(\omega/\omega_0)$	$\tan^{-1}(\omega_0/\omega)$
Transmission at $\omega=0$ (dc)	K	0
Transmission at $\omega=\infty$	0	K
3-dB Frequency	$\omega_0 = 1/\tau$; $\tau \equiv$ time constant $\tau = CR$ or L/R	
Bode Plots	in Fig. 1.23	in Fig. 1.24

Most STC networks can be classified into two categories,[4] **low pass (LP)** and **high pass (HP),** with each of the two categories displaying distinctly different signal responses. As an example, the STC network shown in Fig. 1.22(a) is of the *low-pass* type and that in Fig. 1.22(b) is of the *high-pass* type. To see the reasoning behind this classification, observe that the transfer function of each of these two circuits can be expressed as a voltage-divider ratio, with the divider composed of a resistor and a capacitor. Now, recalling how the impedance of a capacitor varies with frequency ($Z = 1/j\omega C$) it is easy to see that the transmission of the circuit in Fig. 1.22(a) will decrease with frequency and approach zero as ω approaches ∞. Thus the circuit of Fig. 1.22(a) acts as a **low-pass filter;**[5] it passes low-frequency sine-wave inputs with little or no attenuation (at $\omega = 0$, the transmission is unity) and attenuates high-frequency input sinusoids. The circuit of Fig. 1.22(b) does the opposite; its transmission is unity at $\omega = \infty$ and decreases as ω is reduced, reaching 0 for $\omega = 0$. The latter circuit, therefore, performs as a **high-pass filter.**

Table 1.2 provides a summary of the frequency response results for STC networks of both types.[6] Also, sketches of the magnitude and phase responses are given in Figs. 1.23 and 1.24.

[4] An important exception is the *all-pass* STC network studied in Chapter 11.

[5] A filter is a circuit that passes signals in a specified frequency band (the filter passband) and stops or severely attenuates (filters out) signals in another frequency band (the filter stopband). Filters will be studied in Chapter 12.

[6] The transfer functions in Table 1.2 are given in general form. For the circuits of Fig. 1.22, $K = 1$ and $\omega_0 = 1/CR$.

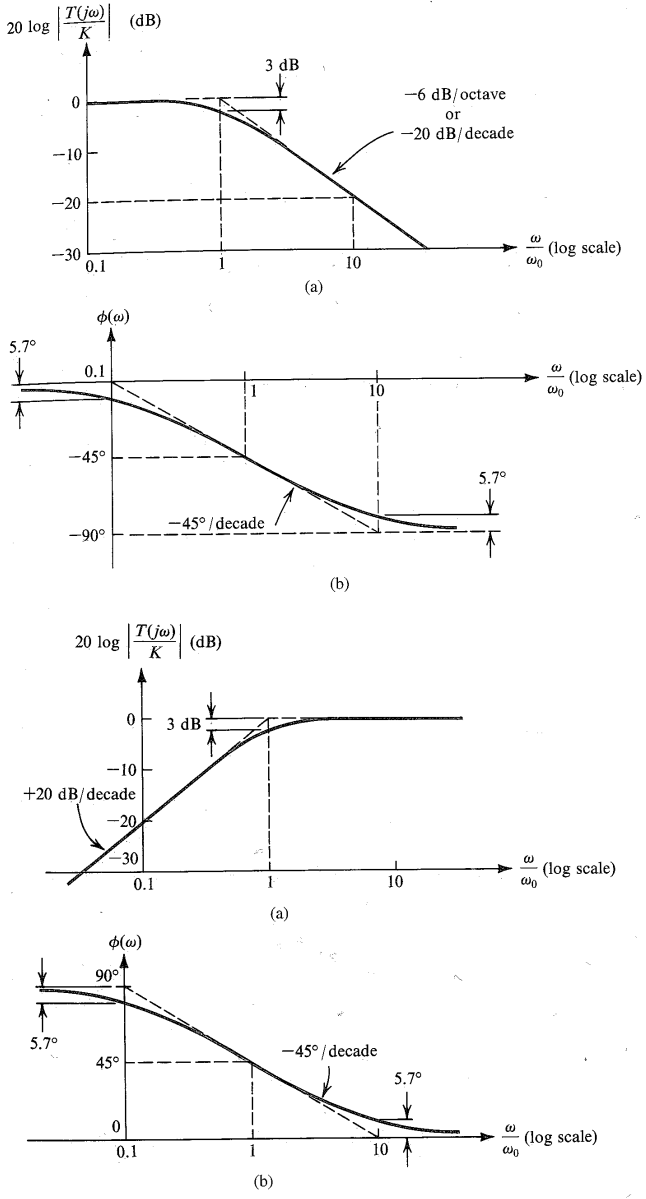


FIGURE 1.23 **(a)** Magnitude and **(b)** phase response of STC networks of the low-pass type.

FIGURE 1.24 **(a)** Magnitude and **(b)** phase response of STC networks of the high-pass type.

These frequency response diagrams are known as **Bode plots** and the **3-dB frequency** (ω_0) is also known as the **corner frequency** or **break frequency.** The reader is urged to become familiar with this information and to consult Appendix D if further clarifications are needed. In particular, it is important to develop a facility for the rapid determination of the time constant τ of an STC circuit.

EXAMPLE 1.5

Figure 1.25 shows a voltage amplifier having an input resistance R_i, an input capacitance C_i, a gain factor μ, and an output resistance R_o. The amplifier is fed with a voltage source V_s having a source resistance R_s, and a load of resistance R_L is connected to the output.

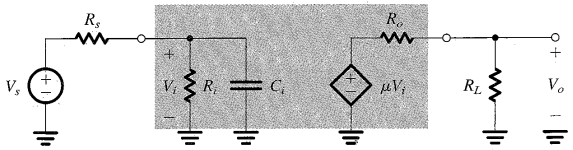


FIGURE 1.25 Circuit for Example 1.5.

(a) Derive an expression for the amplifier voltage gain V_o/V_s as a function of frequency. From this find expressions for the dc gain and the 3-dB frequency.

(b) Calculate the values of the dc gain, the 3-dB frequency, and the frequency at which the gain becomes 0 dB (i.e., unity) for the case $R_s = 20\ \text{k}\Omega$, $R_i = 100\ \text{k}\Omega$, $C_i = 60$ pF, $\mu = 144$ V/V, $R_o = 200\ \Omega$, and $R_L = 1\ \text{k}\Omega$.

(c) Find $v_o(t)$ for each of the following inputs:

(i) $v_i = 0.1 \sin 10^2 t$, V
(ii) $v_i = 0.1 \sin 10^5 t$, V
(iii) $v_i = 0.1 \sin 10^6 t$, V
(iv) $v_i = 0.1 \sin 10^8 t$, V

Solution

(a) Utilizing the voltage-divider rule, we can express V_i in terms of V_s as follows

$$V_i = V_s \frac{Z_i}{Z_i + R_s}$$

where Z_i is the amplifier input impedance. Since Z_i is composed of two parallel elements it is obviously easier to work in terms of $Y_i = 1/Z_i$. Toward that end we divide the numerator and denominator by Z_i, thus obtaining

$$V_i = V_s \frac{1}{1 + R_s Y_i}$$

$$= V_s \frac{1}{1 + R_s[(1/R_i) + sC_i]}$$

Thus,

$$\frac{V_i}{V_s} = \frac{1}{1 + (R_s/R_i) + sC_iR_s}$$

This expression can be put in the standard form for a low-pass STC network (see the top line of Table 1.2) by extracting $[1 + (R_s/R_i)]$ from the denominator; thus we have

$$\frac{V_i}{V_s} = \frac{1}{1 + (R_s/R_i)} \frac{1}{1 + sC_i[(R_sR_i)/(R_s + R_i)]} \tag{1.20}$$

At the output side of the amplifier we can use the voltage-divider rule to write

$$V_o = \mu V_i \frac{R_L}{R_L + R_o}$$

This equation can be combined with Eq. (1.20) to obtain the amplifier transfer function as

$$\frac{V_o}{V_s} = \mu \frac{1}{1 + (R_s/R_i)} \frac{1}{1 + (R_o/R_L)} \frac{1}{1 + sC_i[(R_sR_i)/(R_s + R_i)]} \tag{1.21}$$

We note that only the last factor in this expression is new (compared with the expression derived in the last section). This factor is a result of the input capacitance C_i, with the time constant being

$$\tau = C_i \frac{R_sR_i}{R_s + R_i} \tag{1.22}$$
$$= C_i(R_s // R_i)$$

We could have obtained this result by inspection: From Fig. 1.25 we see that the input circuit is an STC network and that its time constant can be found by reducing V_s to zero, with the result that the resistance seen by C_i is R_i in parallel with R_s. The transfer function in Eq. (1.21) is of the form $K/(1 + (s/\omega_0))$, which corresponds to a low-pass STC network. The dc gain is found as

$$K \equiv \frac{V_o}{V_s}(s = 0) = \mu \frac{1}{1 + (R_s/R_i)} \frac{1}{1 + (R_o/R_L)} \tag{1.23}$$

The 3-dB frequency ω_0 can be found from

$$\omega_0 = \frac{1}{\tau} = \frac{1}{C_i(R_s // R_i)} \tag{1.24}$$

Since the frequency response of this amplifier is of the low-pass STC type, the Bode plots for the gain magnitude and phase will take the form shown in Fig. 1.23, where K is given by Eq. (1.23) and ω_0 is given by Eq. (1.24).

(b) Substituting the numerical values given into Eq. (1.23) results in

$$K = 144 \frac{1}{1 + (20/100)} \frac{1}{1 + (200/1000)} = 100 \text{ V/V}$$

Thus the amplifier has a dc gain of 40 dB. Substituting the numerical values into Eq. (1.24) gives the 3-dB frequency

$$\omega_0 = \frac{1}{60\ \text{pF} \times (20\ \text{k}\Omega // 100\ \text{k}\Omega)}$$
$$= \frac{1}{60 \times 10^{-12} \times (20 \times 100/(20 + 100)) \times 10^3} = 10^6 \text{ rad/s}$$

Thus,

$$f_0 = \frac{10^6}{2\pi} = 159.2 \text{ kHz}$$

Since the gain falls off at the rate of –20 dB/decade, starting at ω_0 (see Fig. 1.23a) the gain will reach 0 dB in two decades (a factor of 100); thus we have

$$\text{Unity-gain frequency} = 100 \times \omega_0 = 10^8 \text{ rad/s or } 15.92 \text{ MHz}$$

(c) To find $v_o(t)$ we need to determine the gain magnitude and phase at 10^2, 10^5, 10^6, and 10^8 rad/s. This can be done either approximately utilizing the Bode plots of Fig. 1.23 or exactly utilizing the expression for the amplifier transfer function,

$$T(j\omega) \equiv \frac{V_o}{V_s}(j\omega) = \frac{100}{1 + j(\omega/10^6)}$$

We shall do both:

(i) For $\omega = 10^2$ rad/s, which is $(\omega_0/10^4)$, the Bode plots of Fig. 1.23 suggest that $|T| \simeq K = 100$ and $\phi = 0°$. The transfer function expression gives $|T| \simeq 100$ and $\phi = -\tan^{-1} 10^{-4} \simeq 0°$. Thus,

$$v_o(t) = 10 \sin 10^2 t, \text{ V}$$

(ii) For $\omega = 10^5$ rad/s, which is $(\omega_0/10)$, the Bode plots of Fig. 1.23 suggest that $|T| \simeq K = 100$ and $\phi = -5.7°$. The transfer function expression gives $|T| = 99.5$ and $\phi = -\tan^{-1} 0.1 = -5.7°$. Thus,

$$v_o(t) = 9.95 \sin(10^5 t - 5.7°), \text{ V}$$

(iii) For $\omega = 10^6$ rad/s $= \omega_0$, $|T| = 100/\sqrt{2} = 70.7$ V/V or 37 dB and $\phi = -45°$. Thus,

$$v_o(t) = 7.07 \sin(10^6 t - 45°), \text{ V}$$

(iv) For $\omega = 10^8$ rad/s, which is $(100\omega_0)$, the Bode plots suggest that $|T| = 1$ and $\phi = -90°$. The transfer function expression gives

$$|T| \simeq 1 \quad \text{and} \quad \phi = -\tan^{-1} 100 = -89.4°,$$

Thus,

$$v_o(t) = 0.1 \sin(10^8 t - 89.4°), \text{ V}$$

1.6.5 Classification of Amplifiers Based on Frequency Response

Amplifiers can be classified based on the shape of their magnitude-response curve. Figure 1.26 shows typical frequency response curves for various amplifier types. In Fig. 1.26(a) the gain remains constant over a wide frequency range but falls off at low and high frequencies. This is a common type of frequency response found in audio amplifiers.

As will be shown in later chapters, **internal capacitances** in the device (a transistor) cause the falloff of gain at high frequencies, just as C_i did in the circuit of Example 1.5. On the other hand, the falloff of gain at low frequencies is usually caused by **coupling capacitors** used to connect one amplifier stage to another, as indicated in Fig. 1.27. This practice is usually adopted to simplify the design process of the different stages. The coupling capacitors are usually chosen quite large (a fraction of a microfarad to a few tens of microfarads) so that their reactance (impedance) is small at the frequencies of interest. Nevertheless, at sufficiently low frequencies the reactance of a coupling capacitor will become large enough to cause part of the signal being coupled to appear as a voltage drop across the coupling capacitor and thus not reach the subsequent stage. Coupling capacitors will thus cause loss of gain at low frequencies and cause the gain to be zero at dc. This is not at all surprising since from Fig. 1.27 we observe that the coupling capacitor, acting together with the input resistance of the subsequent stage, forms a

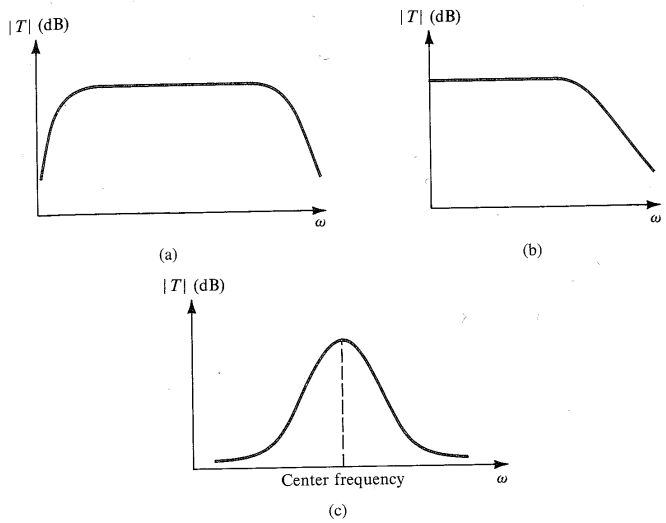


FIGURE 1.26 Frequency response for **(a)** a capacitively coupled amplifier, **(b)** a direct-coupled amplifier, and **(c)** a tuned or bandpass amplifier.

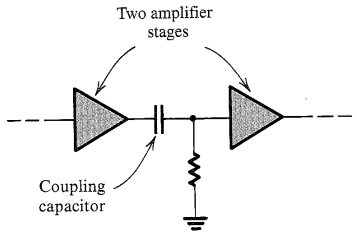


FIGURE 1.27 Use of a capacitor to couple amplifier stages.

high-pass STC circuit. It is the frequency response of this high-pass circuit that accounts for the shape of the amplifier frequency response in Fig. 1.26(a) at the low-frequency end.

There are many applications in which it is important that the amplifier maintain its gain at low frequencies down to dc. Furthermore, monolithic integrated-circuit (IC) technology does not allow the fabrication of large coupling capacitors. Thus IC amplifiers are usually designed as **directly coupled** or **dc amplifiers** (as opposed to **capacitively coupled** or **ac amplifiers**). Figure 1.26(b) shows the frequency response of a dc amplifier. Such a frequency response characterizes what is referred to as a **low-pass amplifier.**

In a number of applications, such as in the design of radio and TV receivers, the need arises for an amplifier whose frequency response peaks around a certain frequency (called the **center frequency**) and falls off on both sides of this frequency, as shown in Fig. 1.26(c).

Amplifiers with such a response are called **tuned amplifiers, bandpass amplifiers,** or **bandpass filters.** A tuned amplifier forms the heart of the front-end or tuner of a communication receiver; by adjusting its center frequency to coincide with the frequency of a desired communications channel (e.g., a radio station), the signal of this particular channel can be received while those of other channels are attenuated or filtered out.

EXERCISES

1.21 Consider a voltage amplifier having a frequency response of the low-pass STC type with a dc gain of 60 dB and a 3-dB frequency of 1000 Hz. Find the gain in dB at $f = 10$ Hz, 10 kHz, 100 kHz, and 1 MHz.

Ans. 60 dB; 40 dB; 20 dB; 0 dB

D1.22 Consider a transconductance amplifier having the model shown in Table 1.1 with $R_i = 5\ \text{k}\Omega$, $R_o = 50\ \text{k}\Omega$, and $G_m = 10$ mA/V. If the amplifier load consists of a resistance R_L in parallel with a capacitance C_L, convince yourself that the voltage transfer function realized, V_o/V_i, is of the low-pass STC type. What is the lowest value that R_L can have while a dc gain of at least 40 dB is obtained? With this value of R_L connected, find the highest value that C_L can have while a 3-dB bandwidth of at least 100 kHz is obtained.

Ans. 12.5 kΩ; 159.2 pF

D1.23 Consider the situation illustrated in Fig. 1.27. Let the output resistance of the first voltage amplifier be 1 kΩ and the input resistance of the second voltage amplifier (including the resistor shown) be 9 kΩ. The resulting equivalent circuit is shown in Fig. E1.23 where V_s and R_s are the output voltage and output resistance of the first amplifier, C is a coupling capacitor, and R_i is the input resistance of the second amplifier. Convince yourself that V_2/V_s is a high-pass STC function. What is the smallest value for C that will ensure that the 3-dB frequency is not higher than 100 Hz?

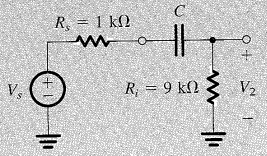


FIGURE E1.23

Ans. 0.16 μF

1.7 DIGITAL LOGIC INVERTERS[7]

The logic inverter is the most basic element in digital circuit design; it plays a role parallel to that of the amplifier in analog circuits. In this section we provide an introduction to the logic inverter.

1.7.1 Function of the Inverter

As its name implies, the logic inverter inverts the logic value of its input signal. Thus for a logic 0 input, the output will be a logic 1, and vice versa. In terms of voltage levels, consider

[7] If desired, study of this section can be postponed to just before study of the CMOS inverter (see Section 4.10).

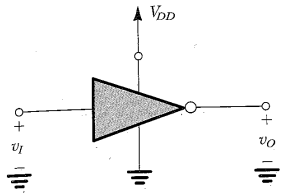


FIGURE 1.28 A logic inverter operating from a dc supply V_{DD}.

the inverter shown in block form in Fig. 1.28: When v_I is low (close to 0 V), the output v_O will be high (close to V_{DD}), and vice versa.

1.7.2 The Voltage Transfer Characteristic (VTC)

To quantify the operation of the inverter, we utilize its voltage transfer characteristic (VTC, as it is usually abbreviated). First we refer the reader to the amplifier considered in Example 1.2 whose transfer characteristic is sketched in Fig. 1.15. Observe that the transfer characteristic indicates that this inverting amplifier can be used as a logic inverter. Specifically, if the input is high ($v_I > 0.690$ V), v_O will be low at 0.3 V. On the other hand, if the input is low (close to 0 V), the output will be high (close to 10 V). Thus to use this amplifier as a logic inverter, we utilize its extreme regions of operation. This is exactly the opposite to its use as a signal amplifier, where it would be biased at the middle of the transfer characteristic and the signal kept sufficiently small so as to restrict operation to a short, almost linear, segment of the transfer curve. Digital applications, on the other hand, make use of the gross nonlinearity exhibited by the VTC.

With these observations in mind, we show in Fig. 1.29 a possible VTC of a logic inverter. For simplicity, we are using three straight lines to approximate the VTC, which is usually a nonlinear curve such as that in Fig. 1.15. Observe that the output high level,

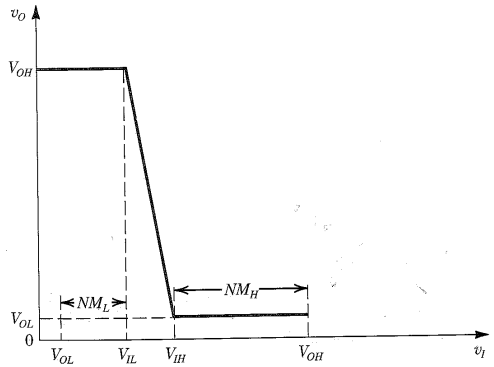


FIGURE 1.29 Voltage transfer characteristic of an inverter. The VTC is approximated by three straight-line segments. Note the four parameters of the VTC (V_{OH}, V_{OL}, V_{IL}, and V_{IH}) and their use in determining the noise margins (NM_H and NM_L).

denoted V_{OH}, does not depend on the exact value of v_I as long as v_I does not exceed the value labeled V_{IL}; when v_I exceeds V_{IL}, the output decreases and the inverter enters its amplifier region of operation, also called the **transition region.** It follows that V_{IL} is an important parameter of the inverter VTC: It is the *maximum value that v_I can have while being interpreted by the inverter as representing a logic 0.*

Similarly, we observe that the output low level, denoted V_{OL}, does not depend on the exact value of v_I as long as v_I does not fall below V_{IH}. Thus V_{IH} is an important parameter of the inverter VTC: It is the *minimum value that v_I can have while being interpreted by the inverter as representing a logic 1.*

1.7.3 Noise Margins

The insensitivity of the inverter output to the exact value of v_I within allowed regions is a great advantage that digital circuits have over analog circuits. To quantify this insensitivity property, consider the situation that occurs often in a digital system where an inverter (or a logic gate based on the inverter circuit) is driving another similar inverter. If the output of the driving inverter is high at V_{OH}, we see that we have a "margin of safety" equal to the difference between V_{OH} and V_{IH} (see Fig. 1.29). In other words, if for some reason a disturbing signal (called "electric noise," or simply **noise**) is superimposed on the output of the driving inverter, the driven inverter would not be "bothered" so long as this noise does not decrease the voltage at its input below V_{IH}. Thus we can say that the inverter has a **noise margin for high input,** NM_H, of

$$NM_H = V_{OH} - V_{IH} \tag{1.25}$$

Similarly, if the output of the driving inverter is low at V_{OL}, the driven inverter will provide a high output even if noise corrupts the V_{OL} level at its input, raising it up to nearly V_{IL}. Thus we can say that the inverter exhibits a **noise margin for low input,** NM_L, of

$$NM_L = V_{IL} - V_{OL} \tag{1.26}$$

In summary, four parameters, V_{OH}, V_{OL}, V_{IH}, and V_{IL}, define the VTC of an inverter and determine its noise margins, which in turn measure the ability of the inverter to tolerate variations in the input signal levels. In this regard, observe that changes in the input signal level within the noise margins are *rejected* by the inverter. Thus noise is not allowed to propagate further through the system, a definite advantage of digital over analog circuits. Alternatively, we can think of the inverter as *restoring* the signal levels to standard values (V_{OL} and V_{OH}) even when it is presented with corrupted signal levels (within the noise margins). As a summary, useful for future reference, we present a listing of the definitions of the important parameters of the inverter VTC in Table 1.3.

TABLE 1.3 Important Parameters of the VTC of the Logic Inverter (Refer to Fig. 1.29)

V_{OL}: Output low level
V_{OH}: Output high level
V_{IL}: Maximum value of input interpreted by the inverter as a logic 0
V_{IH}: Minimum value of input interpreted by the inverter as a logic 1
NM_L: Noise margin for low input = $V_{IL} - V_{OL}$
NM_H: Noise margin for high input = $V_{OH} - V_{IH}$

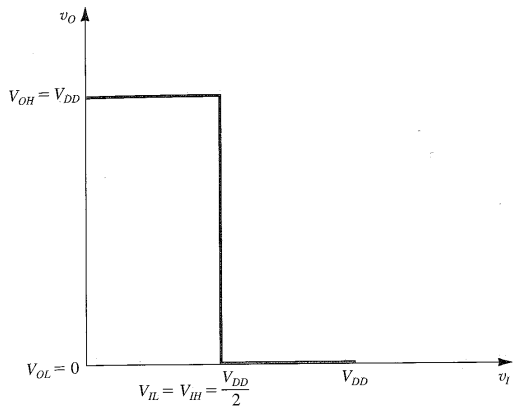


FIGURE 1.30 The VTC of an ideal inverter.

1.7.4 The Ideal VTC

The question naturally arises as to what constitutes an ideal VTC for an inverter. The answer follows directly from the preceding discussion: An ideal VTC is one that maximizes the noise margins and distributes them equally between the low and high input regions. Such a VTC is shown in Fig. 1.30 for an inverter operated from a dc supply V_{DD}. Observe that the output high level V_{OH} is at its maximum possible value of V_{DD}, and the output low level is at its minimum possible value of 0 V. Observe also that the threshold voltages V_{IL} and V_{IH} are equalized and placed at the middle of the power supply voltage ($V_{DD}/2$). Thus the width of the transition region between the high and low output regions has been reduced to zero. The transition region, though obviously very important for amplifier applications, is of no value in digital circuits. The ideal VTC exhibits a steep transition at the threshold voltage $V_{DD}/2$ with the gain in the transition region being infinite. The noise margins are now equal:

$$NM_H = NM_L = V_{DD}/2 \tag{1.27}$$

We will see in Chapter 4 that inverter circuits designed using the complementary metal-oxide-semiconductor (or CMOS) technology come very close to realizing the ideal VTC.

1.7.5 Inverter Implementation

Inverters are implemented using transistors (Chapters 4 and 5) operating as **voltage-controlled switches.** The simplest inverter implementation is shown in Fig. 1.31. The switch is controlled by the inverter input voltage v_I: When v_I is low, the switch will be open and $v_O = V_{DD}$ since no current flows through R. When v_I is high, the switch will be closed and, assuming an ideal switch, $v_O = 0$.

Transistor switches, however, as we will see in Chapters 4 and 5, are not perfect. Although their **off resistances** are very high and thus an open switch closely approximates

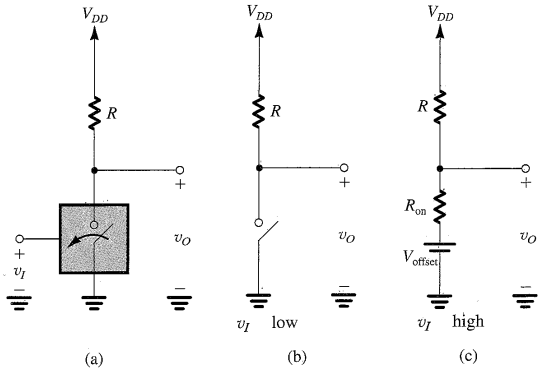


FIGURE 1.31 **(a)** The simplest implementation of a logic inverter using a voltage-controlled switch; **(b)** equivalent circuit when v_I is low; and **(c)** equivalent circuit when v_I is high. Note that the switch is assumed to close when v_I is high.

an open circuit, the "on" switch has a finite closure or **"on" resistance,** R_{on}. Furthermore, some switches (e.g., those implemented using bipolar transistors; see Chapter 5) exhibit in addition to R_{on} an **offset voltage,** V_{offset}. The result is that when v_I is high, the inverter has the equivalent circuit shown in Fig. 1.31(c), from which V_{OL} can be found.

More elaborate implementations of the logic inverter exist, and we show two of these in Figs. 1.32(a) and 1.33(a). The circuit in Fig. 1.32(a) utilizes a pair of **complementary switches,** the **"pull-up" (PU) switch** connects the output node to V_{DD}, and the **"pull-down" (PD) switch** connects the output node to ground. When v_I is low, the PU switch will be

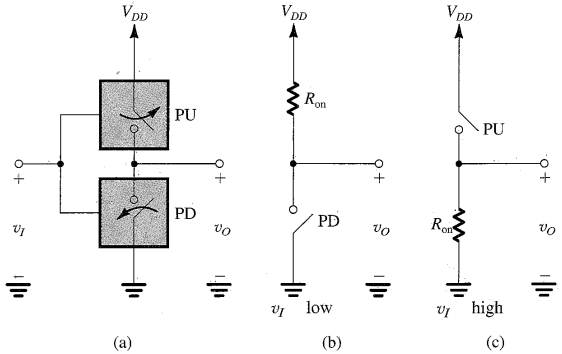


FIGURE 1.32 A more elaborate implementation of the logic inverter utilizing two complementary switches. This is the basis of the CMOS inverter studied in Section 4.10.

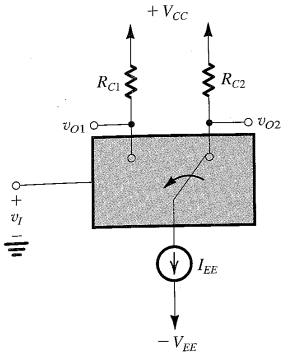


FIGURE 1.33 Another inverter implementation utilizing a double-throw switch to steer the constant current I_{EE} to R_{C1} (when v_I is high) or R_{C2} (when v_I is low). This is the basis of the emitter-coupled logic (ECL) studied in Chapters 7 and 11.

closed and the PD switch open, resulting in the equivalent circuit of Fig. 1.32(b). Observe that in this case R_{on} of PU connects the output to V_{DD}, thus establishing $V_{OH} = V_{DD}$. Also observe that no current flows and thus no power is dissipated in the circuit. Next, if v_I is raised to the logic 1 level, the PU switch will open while the PD switch will close, resulting in the equivalent circuit shown in Fig. 1.32(c). Here R_{on} of the PD switch connects the output to ground, thus establishing $V_{OL} = 0$. Here again no current flows, and no power is dissipated. The superiority of this implementation over that using the single pull-down switch and a resistor (known as a pull-up resistor) should be obvious. This circuit constitutes the basis of the CMOS inverter that we will study in Section 4.10. Note that we have not included offset voltages in the equivalent circuits because MOS switches do not exhibit a voltage offset (Chapter 4).

Finally, consider the inverter implementation of Fig. 1.33. Here a double-throw switch is used to steer the constant current I_{EE} into one of two resistors connected to the positive supply V_{CC}. The reader is urged to show that if a high v_I results in the switch being connected to R_{C1}, then a logic inversion-function is realized at v_{O1}. Note that the output voltage is independent of the switch resistance. This *current-steering* or *current-mode* logic arrangement is the basis of the fastest available digital logic circuits, called emitter-coupled logic (ECL), introduced in Chapter 7 and studied in Chapter 11.

1.7.6 Power Dissipation

Digital systems are implemented using very large numbers of logic gates. For space and other economic considerations, it is desirable to implement the system with as few integrated-circuit (IC) chips as possible. It follows that one must pack as many logic gates as possible on an IC chip. At present, 100,000 gates or more can be fabricated on a single IC chip in what is known as **very-large-scale integration (VLSI).** To keep the power dissipated in the chip to acceptable limits (imposed by thermal considerations), the power dissipation per gate must be kept to a minimum. Indeed, a very important performance measure of the logic inverter is the power it dissipates.

The simple inverter of Fig. 1.31 obviously dissipates no power when v_I is low and the switch is open. In the other state, however, the power dissipation is approximately V_{DD}^2/R and can be substantial. This power dissipation occurs even if the inverter is not switching

and is thus known as **static power dissipation.** The inverter of Fig. 1.32 exhibits no static power dissipation, a definite advantage. Unfortunately, however, another component of power dissipation arises when a capacitance exists between the output node of the inverter and ground. This is always the case, for the devices that implement the switches have internal capacitances, the wires that connect the inverter output to other circuits have capacitance, and, of course, there is the input capacitance of whatever circuit the inverter is driving. Now, as the inverter is switched from one state to another, current must flow through the switch(es) to charge (and discharge) the load capacitance. These currents give rise to power dissipation in the switches, called **dynamic power dissipation.** In Chapter 4, we shall study dynamic power dissipation in the CMOS inverter, and we shall show that an inverter switched at a frequency f Hz exhibits a dynamic power dissipation

$$P_{\text{dynamic}} = fCV_{DD}^2 \tag{1.28}$$

where C is the capacitance between the output node and ground and V_{DD} is the power-supply voltage. This result applies (approximately) to all inverter circuits.

1.7.7 Propagation Delay

Whereas the dynamic behavior of amplifiers is specified in terms of their frequency response, that of inverters is characterized in terms of the time delay between switching of v_I (from low to high or vice versa) and the corresponding change appearing at the output. Such a delay, called **propagation delay,** arises for two reasons: The transistors that implement the switches exhibit finite (nonzero) switching times, and the capacitance that is inevitably present between the inverter output node and ground needs to charge (or discharge, as the case may be) before the output reaches its required level of V_{OH} or V_{OL}. We shall analyze the inverter switching times in subsequent chapters. Such a study depends on a thorough familiarity with the time response of single-time-constant (STC) circuits. A review of this subject is presented in Appendix D. For our purposes here, we remind the reader of the key equation in determining the response to a step function:

Consider a step-function input applied to an STC network of either the low-pass or high-pass type, and let the network have a time constant τ. The output at any time t is given by

$$y(t) = Y_\infty - (Y_\infty - Y_{0+})e^{-t/\tau} \tag{1.29}$$

where Y_∞ is the final value, that is, the value toward which the response is heading, and Y_{0+} is the value of the response immediately after $t = 0$. This equation states that the output at any time t is equal to the difference between the final value Y_∞ and a gap whose initial value is $Y_\infty - Y_{0+}$ and that is shrinking exponentially.

EXAMPLE 1.6

Consider the inverter of Fig. 1.31(a) with a capacitor $C = 10$ pF connected between the output and ground. Let $V_{DD} = 5$ V, $R = 1$ kΩ, $R_{\text{on}} = 100$ Ω, and $V_{\text{offset}} = 0.1$ V. If at $t = 0$, v_I goes low and neglecting the delay time of the switch, that is, assuming that it opens immediately, find the time for the output to reach $\frac{1}{2}(V_{OH} + V_{OL})$. The time to this 50% point on the output waveform is defined as the low-to-high propagation delay, t_{PLH}.

Solution

First we determine V_{OL}, which is the voltage at the output prior to $t = 0$. From the equivalent circuit in Fig. 1.31(b), we find

$$V_{OL} = V_{\text{offset}} + \frac{V_{DD} - V_{\text{offset}}}{R + R_{\text{on}}} R_{\text{on}}$$

$$= 0.1 + \frac{5 - 0.1}{1.1} \times 0.1 = 0.55 \text{ V}$$

Next, when the switch opens at $t = 0$, the circuit takes the form shown in Fig. 1.34(a). Since the voltage across the capacitor cannot change instantaneously, at $t = 0+$ the output will still be 0.55 V.

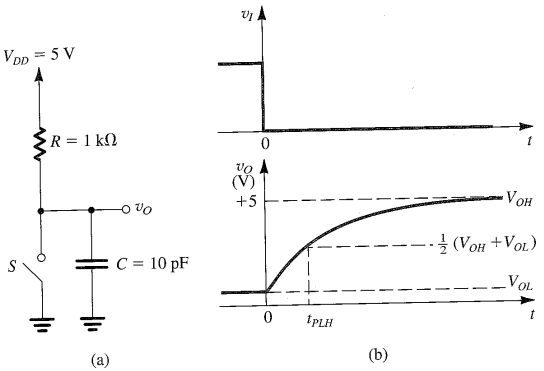


FIGURE 1.34 Example 1.6: **(a)** The inverter circuit after the switch opens (i.e., for $t \geq 0+$). **(b)** Waveforms of v_I and v_O. Observe that the switch is assumed to operate instantaneously. v_O rises exponentially, starting at V_{OL} and heading toward V_{OH}.

Then the capacitor charges through R, and v_O rises exponentially toward V_{DD}. The output waveform will be as shown in Fig. 1.34(b), and its equation can be obtained by substituting in Eq. (1.29), $v_O(\infty) = 5$ V and $v_O(0+) = 0.55$ V. Thus,

$$v_O(t) = 5 - (5 - 0.55)e^{-t/\tau}$$

where $\tau = CR$. To find t_{PLH}, we substitute

$$v_O(t_{PLH}) = \tfrac{1}{2}(V_{OH} + V_{OL})$$

$$= \tfrac{1}{2}(5 + 0.55)$$

The result is

$$t_{PLH} = 0.69\tau$$

$$= 0.69RC$$

$$= 0.69 \times 10^3 \times 10^{-11}$$

$$= 6.9 \text{ ns}$$

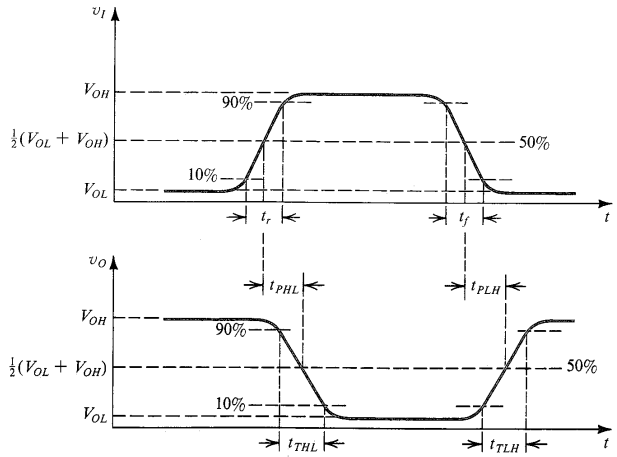


FIGURE 1.35 Definitions of propagation delays and transition times of the logic inverter.

We conclude this section by showing in Fig. 1.35 the formal definition of the propagation delay of an inverter. As shown, an input pulse with finite (nonzero) **rise and fall times** is applied. The inverted pulse at the output exhibits finite rise and fall times (labeled t_{TLH} and t_{THL}, where the subscript T denotes transition, LH denotes low-to-high, and HL denotes high-to-low). There is also a delay time between the input and output wave forms. The usual way to specify the propagation delay is to take the average of the high-to-low propagation delay, t_{PHL}, and the low-to-high propagation delay, t_{PLH}. As indicated, these delays are measured between the 50% points of the input and output waveforms. Also note that the transition times are specified using the 10% and 90% points of the output excursion ($V_{OH} - V_{OL}$).

EXERCISES

1.24 For the inverter in Fig. 1.31, let $V_{DD} = 5$ V, $R = 1$ kΩ, $R_{on} = 100\ \Omega$, $V_{offset} = 0.1$ V, $V_{IL} = 0.8$ V, and $V_{iH} = 1.2$ V. Find V_{OH}, V_{OL}, NM_H, and NM_L. Also find the average static power dissipation assuming that the inverter spends half the time in each of its two states.

Ans. 5 V; 0.55 V; 3.8 V; 0.25 V; 11.1 mW

1.25 Find the dynamic power dissipated in an inverter operated from a 5-V power supply. The inverter has a 2-pF capacitance load and is switched at 50 MHz.

Ans. 2.5 mW

1.8 CIRCUIT SIMULATION USING SPICE

The use of computer programs to simulate the operation of electronic circuits has become an essential step in the circuit-design process. This is especially the case for circuits that are to be fabricated in integrated-circuit form. However, even circuits that are assembled on a printed-circuit board using discrete components can and do benefit from circuit simulation. Circuit simulation enables the designer to verify that the design will meet specifications when actual components (with their many imperfections) are used, and it can also provide additional insight into circuit operation allowing the designer to fine-tune the final design prior to fabrication. However, notwithstanding the advantages of computer simulation, it is not a substitute for a thorough understanding of circuit operation. It should be performed only at a later stage in the design process and, most certainly, after a paper-and-pencil design has been done.

Among the various circuit-simulation programs available for the computer-aided numerical analysis of microelectronic circuits, **SPICE** (*S*imulation *P*rogram with *I*ntegrated *C*ircuit *E*mphasis) is generally regarded to be the most widely used. SPICE is an open-source program which has been under development by the University of California at Berkeley since the early 1970s. **PSpice** is a commercial personal-computer version of SPICE that is now commercially available from Cadence. Also available from Cadence is **PSpice A/D**—an advanced version of PSpice that can model the behavior and, hence, simulate circuits that process a mix of both analog and digital signals.[8] SPICE was originally a text-based program: The user had to describe the circuit to be simulated and the type of simulation to be performed using an input text file, called a **netlist.** The simulation results were also displayed as text. As an example of more recent developments, Cadence provides a graphical interface, called **OrCAD Capture CIS** (Component *I*nformation *S*ystem), for circuit-schematic entry and editing. Such graphical interface tools are referred to in the literature as **schematic entry, schematic editor,** or **schematic capture** tools. Furthermore, PSpice A/D includes a graphical postprocessor, called **Probe,** to numerically analyze and graphically display the results of the PSpice simulations. In this text, **"using PSpice"** or **"using SPICE"** loosely refers to using Capture CIS, PSpice A/D, and Probe to simulate a circuit and to numerically analyze and graphically display the simulation results.

An evaluation (student) version of Capture CIS and PSpice A/D are included on the CD accompanying this book. These correspond to the OrCAD Family Release 9.2 Lite Edition available from Cadence. Furthermore, the circuit diagrams entered in Capture CIS (called **Capture Schematics**) and the corresponding PSpice simulation files of all SPICE examples in this book can be found on the text's CD and website (www.sedrasmith.org). Access to these files will allow the reader to undertake further experimentation with these circuits, including investigating the effect of changing component values and operating conditions.

It is not our objective in this book to teach the reader *how* SPICE works nor the intricacies of using it effectively. This can be found in the SPICE books listed in Appendix F. Our objective in the sections of this book devoted to SPICE, usually the last section of each chapter, is twofold: to describe the models that are used by SPICE to represent the various electronic devices, and to illustrate how useful SPICE can be in investigating circuit operation.

[8] Such circuits are called mixed-signal circuits, and the simulation programs that can simulate such circuits are called mixed-signal simulators.

SUMMARY

- An electrical signal source can be represented in either the Thévenin form (a voltage source v_s in series with a source resistance R_s) or the Norton form (a current source i_s in parallel with a source resistance R_s). The Thévenin voltage v_s is the open-circuit voltage between the source terminals; equal to the Norton current i_s is equal to the short-circuit current between the source terminals. For the two representations to be equivalent, $v_s = R_s i_s$.
- The sine-wave signal is completely characterized by its peak value (or rms value which is the peak $/\sqrt{2}$), its frequency (ω in rad/s or f in Hz; $\omega = 2\pi f$ and $f = 1/T$ where T is the period in seconds), and its phase with respect to an arbitrary reference time.
- A signal can be represented either by its waveform versus time, or as the sum of sinusoids. The latter representation is known as the frequency spectrum of the signal.
- Analog signals have magnitudes that can assume any value. Electronic circuits that process analog signals are called analog circuits. Sampling the magnitude of an analog signal at discrete instants of time and representing each signal sample by a number, results in a digital signal. Digital signals are processed by digital circuits.
- The simplest digital signals are obtained when the binary system is used. An individual digital signal then assumes one of only two possible values: low and high (say, 0 V and +5 V), corresponding to logic 0 and logic 1, respectively.
- An analog-to-digital converter (ADC) provides at its output the digits of the binary number representing the analog signal sample applied to its input. The output digital signal can then be processed using digital circuits. Refer to Fig. 1.9 and Eq. 1.3.
- The transfer characteristic, v_O versus v_I, of a linear amplifier is a straight line with a slope equal to the voltage gain. Refer to Fig. 1.11.
- Amplifiers increase the signal power and thus require dc power supplies for their operation.
- The amplifier voltage gain can be expressed as a ratio A_v in V/V or in decibels, 20 log$|A_v|$, dB. Similarly, for current gain: A_i A/A or 20 log$|A_i|$, dB. For power gain: A_p W/W or 10 log A_p, dB.
- Linear amplification can be obtained from a device having a nonlinear transfer characteristic by employing dc biasing and keeping the input signal amplitude small. Refer to Fig. 1.14.
- Depending on the signal to be amplified (voltage or current) and on the desired form of output signal (voltage or current), there are four basic amplifier types: voltage, current, transconductance, and transresistance amplifiers. For the circuit models and ideal characteristics of these four amplifier types, refer to Table 1.1. A given amplifier can be modeled by any one of the four models, in which case their parameters are related by the formulas in Eqs. (1.14) to (1.16).
- A sinusoid is the only signal whose wave form is unchanged through a linear circuit. Sinusoidal signals are used to measure the frequency response of amplifiers.
- The transfer function $T(s) \equiv V_o(s)/V_i(s)$ of a voltage amplifier can be determined from circuit analysis. Substituting $s = j\omega$ gives $T(j\omega)$, whose magnitude $|T(j\omega)|$ is the magnitude response, and whose phase $\phi(\omega)$ is the phase response, of the amplifier.
- Amplifiers are classified according to the shape of their frequency response, $|T(j\omega)|$. Refer to Fig. 1.26.
- Single-time-constant (STC) networks are those networks that are composed of, or can be reduced to, one reactive component (L or C) and one resistance (R). The time constant τ is either L/R or CR.
- STC networks can be classified into two categories: low-pass (LP) and high-pass (HP). LP networks pass dc and low frequencies and attenuate high frequencies. The opposite is true for HP networks.
- The gain of an LP (HP) STC circuit drops by 3 dB below the zero-frequency (infinite-frequency) value at a frequency $\omega_0 = 1/\tau$. At high frequencies (low frequencies) the gain falls off at the rate of 6 dB/octave or 20 dB/decade. Refer to Table 1.2 on page 34 and Figs. (1.23) and (1.24). Further details are given in Appendix E.
- The digital logic inverter is the basic building block of digital circuits, just as the amplifier is the basic building block of analog circuits.
- The static operation of the inverter is described by its voltage transfer characteristic (VTC). The break-points of the transfer characteristic determine the inverter noise margins; refer to Fig. 1.29 and Table 1.3. In particular, note that $NM_H = V_{OH} - V_{IH}$ and $NM_L = V_{IL} - V_{OL}$.
- The inverter is implemented using transistors operating as voltage-controlled switches. The arrangement utilizing two switches operated in a complementary fashion results in a high-performance inverter. This is the basis for the CMOS inverter studied in Chapter 4.
- An important performance parameter of the inverter is the amount of power it dissipates. There are two components of power dissipation: static and dynamic. The first is a result of current flow in either the 0 or 1 state or both. The second occurs when the inverter is switched and has a capacitor load. Dynamic power dissipation is given approximately by fCV_{DD}^2.
- Another very important performance parameter of the inverter is its propagation delay (see Fig. 1.35 for definitions).

PROBLEMS[1,2]

CIRCUIT BASICS

As a review of the basics of circuit analysis and in order for the readers to gauge their preparedness for the study of electronic circuits, this section presents a number of relevant circuit analysis problems. For a summary of Thévenin's and Norton's theorems, refer to Appendix D. The problems are grouped in appropriate categories.

RESISTORS AND OHM'S LAW

1.1 Ohm's law relates V, I, and R for a resistor. For each of the situations following, find the missing item:

(a) $R = 1$ kΩ, $V = 10$ V
(b) $V = 10$ V, $I = 1$ mA
(c) $R = 10$ kΩ, $I = 10$ mA
(d) $R = 100$ Ω, $V = 10$ V

1.2 Measurements taken on various resistors are shown below. For each, calculate the power dissipated in the resistor and the power rating necessary for safe operation using standard components with power ratings of 1/8 W, 1/4 W, 1/2 W, 1 W, or 2 W:

(a) 1 kΩ conducting 30 mA
(b) 1 kΩ conducting 40 mA
(c) 10 kΩ conducting 3 mA
(d) 10 kΩ conducting 4 mA
(e) 1 kΩ dropping 20 V
(f) 1 kΩ dropping 11 V

1.3 Ohm's law and the power law for a resistor relate V, I, R, and P, making only two variables independent. For each pair identified below, find the other two:

(a) $R = 1$ kΩ, $I = 10$ mA
(b) $V = 10$ V, $I = 1$ mA
(c) $V = 10$ V, $P = 1$ W
(d) $I = 10$ mA, $P = 0.1$ W
(e) $R = 1$ kΩ, $P = 1$ W

COMBINING RESISTORS

1.4 You are given three resistors whose values are 10 kΩ, 20 kΩ, and 40 kΩ. How many different resistances can you create using series and parallel combinations of these three? List them in value order, lowest first. Be thorough and organized. (*Hint:* In your search, first consider all parallel combinations, then consider series combinations, and then consider series-parallel combinations, of which there are two kinds).

1.5 In the analysis and test of electronic circuits, it is often useful to connect one resistor in parallel with another to obtain a nonstandard value, one which is smaller than the smaller of the two resistors. Often, particularly during circuit testing, one resistor is already installed, in which case the second, when connected in parallel, is said to "shunt" the first. If the original resistor is 10 kΩ, what is the value of the shunting resistor needed to reduce the combined value by 1%, 5%, 10%, and 50%? What is the result of shunting a 10-kΩ resistor by 1 MΩ? By 100 kΩ? By 10 kΩ?

VOLTAGE DIVIDERS

1.6 Figure P1.6(a) shows a two-resistor voltage divider. Its function is to generate a voltage V_O (smaller than the power-supply voltage V_{DD}) at its output node X. The circuit looking back at node X is equivalent to that shown in Fig. P1.6(b). Observe that this is the Thévenin equivalent of the voltage divider circuit. Find expressions for V_O and R_O.

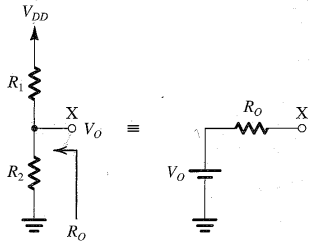


FIGURE P1.6

[1] Somewhat difficult problems are marked with an asterisk (*); more difficult problems are marked with two asterisks (**); and very difficult (and/or time-consuming) problems are marked with three asterisks (***).
[2] Design-oriented problems are marked with a D.

1.7 A two-resistor voltage divider employing a 3.3-kΩ and a 6.8-kΩ resistor is connected to a 9-V ground-referenced power supply to provide a relatively low voltage. Sketch the circuit. Assuming exact-valued resistors, what output voltage (measured to ground) and equivalent output resistance result? If the resistors used are not ideal but have a ±5% manufacturing tolerance, what are the extreme output voltages and resistances that can result?

1.8 You are given three resistors, each of 10 kΩ, and a 9-V battery whose negative terminal is connected to ground. With a voltage divider using some or all of your resistors, how many positive-voltage sources of magnitude less than 9 V can you design? List them in order, smallest first. What is the output resistance (i.e., the Thévenin resistance) of each?

D*1.9 Two resistors, with nominal values of 4.7 kΩ and 10 kΩ, are used in a voltage divider with a +15-V supply to create a nominal +10-V output. Assuming the resistor values to be exact, what is the actual output voltage produced? Which resistor must be shunted (paralleled) by what third resistor to create a voltage-divider output of 10.00 V? If an output resistance of exactly 3.33 kΩ is also required, what do you suggest? What should be done if the requirement is 10.00 V and 3.00 kΩ while still using the original 4.7-kΩ and 10-kΩ resistors?

CURRENT DIVIDERS

1.10 Current dividers play an important role in circuit design. Therefore it is important to develop a facility for dealing with current dividers in circuit analysis. Figure P1.10 shows a two-resistor current divider fed with an ideal current source I. Show that

$$I_1 = \frac{R_2}{R_1 + R_2} I$$

$$I_2 = \frac{R_1}{R_1 + R_2} I$$

and find the voltage V that develops across the current divider.

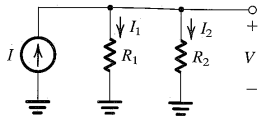


FIGURE P1.10

D1.11 Design a simple current divider that will reduce the current provided to a 1-kΩ load to 20% of that available from the source.

D1.12 A designer searches for a simple circuit to provide one-third of a signal current I to a load resistance R. Suggest a solution using one resistor. What must its value be? What is the input resistance of the resulting current divider? For a particular value R, the designer discovers that the otherwise-best-available resistor is 10% too high. Suggest two circuit topologies using one additional resistor that will solve this problem. What is the value of the resistor required? What is the input resistance of the current divider in each case?

D1.13 A particular electronic signal source generates currents in the range 0 mA to 1 mA under the condition that its load voltage not exceed 1 V. For loads causing more than 1 V to appear across the generator, the output current is no longer assured but will be reduced by some unknown amount. This circuit limitation, occurring, for example, at the peak of a signal sine wave, will lead to undesirable signal distortion that must be avoided. If a 10-kΩ load is to be connected, what must be done? What is the name of the circuit you must use? How many resistors are needed? What is (are) the(ir) value(s)?

THÉVENIN-EQUIVALENT CIRCUITS

1.14 For the circuit in Fig. P1.14, find the Thévenin equivalent circuit between terminals (a) 1 and 2, (b) 2 and 3, and (c) 1 and 3.

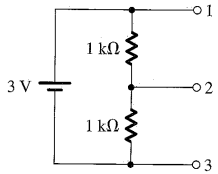


FIGURE P1.14

1.15 Through repeated application of Thévenin's theorem, find the Thévenin-equivalent of the circuit in Fig. P1.15 between node 4 and ground and hence find the current that flows through a load resistance of 1.5 kΩ connected between node 4 and ground.

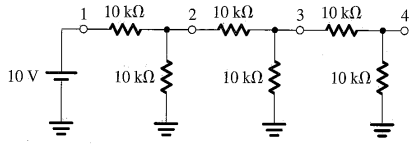


FIGURE P1.15

CIRCUIT ANALYSIS

1.16 For the circuit shown in Fig. P1.16, find the current in all resistors and the voltage (with respect to ground) at their common node using two methods:

(a) Current: Define branch currents I_1 and I_2 in R_1 and R_2, respectively; identify two equations; and solve them.
(b) Voltage: Define the node voltage V at the common node; identify a single equation; and solve it.

Which method do you prefer? Why?

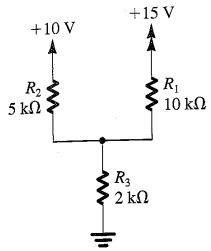


FIGURE P1.16

1.17 The circuit shown in Fig. P1.17 represents the equivalent circuit of an unbalanced bridge. It is required to calculate the current in the detector branch (R_5) and the voltage across it. Although this can be done using loop and node equations, a much easier approach is possible: Find the Thévenin equivalent of the circuit to the left of node 1 and the Thévenin equivalent of the circuit to the right of node 2. Then solve the resulting simplified circuit.

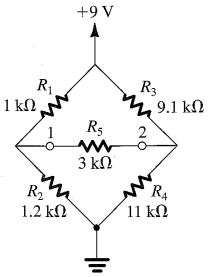


FIGURE P1.17

1.18 For the circuit in Fig. P1.18, find the equivalent resistance to ground, R_{eq}. To do this, apply a voltage V_x between terminal X and ground and find the current drawn from V_x. Note that you can use particular special properties of the circuit to get the result directly! Now, if R_4 is raised to 1.2 kΩ, what does R_{eq} become?

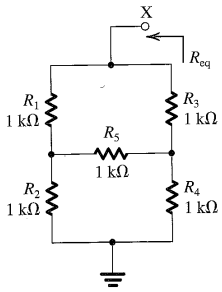


FIGURE P1.18

AC CIRCUITS

1.19 The periodicity of recurrent waveforms, such as sine waves or square waves, can be completely specified using only one of three possible parameters: radian frequency, ω, in radians per second (rad/s); (conventional) frequency, f, in Hertz (Hz); or period T, in seconds (s). As well, each of the parameters can be specified numerically in one of several ways: using letter prefixes associated with the basic units, using scientific notation, or using some combination of both. Thus, for example, a particular period may be specified as 100 ns, 0.1 μs, 10^{-1} μs, 10^5 ps, or 1×10^{-7} s. (For the definition of the various prefixes used in electronics, see Appendix H.) For each of the measures listed below, express the trio of terms in scientific notation associated with the basic unit (e.g., 10^{-7} s rather than 10^{-1} μs).

(a) $T = 10^{-4}$ ms
(b) $f = 1$ GHz
(c) $\omega = 6.28 \times 10^2$ rad/s
(d) $T = 10$ s
(e) $f = 60$ Hz
(f) $\omega = 1$ krad/s
(g) $f = 1900$ MHz

1.20 Find the complex impedance, Z, of each of the following basic circuit elements at 60 Hz, 100 kHz, and 1 GHz:

(a) $R = 1$ kΩ
(b) $C = 10$ nF
(c) $C = 2$ pF
(d) $L = 10$ mH
(e) $L = 1$ nH

1.21 Find the complex impedance at 10 kHz of the following networks:

(a) 1 kΩ in series with 10 nF
(b) 1 kΩ in parallel with 0.01 μF

(c) 100 kΩ in parallel with 100 pF
(d) 100 Ω in series with 10 mH

SECTION 1.1: SIGNALS

1.22 Any given signal source provides an open-circuit voltage, v_{oc}, and a short-circuit current i_{sc}. For the following sources, calculate the internal resistance, R_s; the Norton current, i_s; and the Thévenin voltage, v_s:

(a) $v_{oc} = 10$ V, $i_{sc} = 100$ μA
(b) $v_{oc} = 0.1$ V, $i_{sc} = 10$ μA

1.23 A particular signal source produces an output of 30 mV when loaded by a 100-kΩ resistor and 10 mV when loaded by a 10-kΩ resistor. Calculate the Thévenin voltage, Norton current, and source resistance.

1.24 A temperature sensor is specified to provide 2 mV/°C. When connected to a load resistance of 10 kΩ, the output voltage was measured to change by 10 mV, corresponding to a change in temperature of 10°C. What is the source resistance of the sensor?

1.25 Refer to the Thévenin and Norton representations of the signal source (Fig. 1.1). If the current supplied by the source is denoted i_o and the voltage appearing between the source output terminals is denoted v_o, sketch and clearly label v_o versus i_o for $0 \le i_o \le i_s$.

1.26 The connection of a signal source to an associated signal processor or amplifier generally involves some degree of signal loss as measured at the processor or amplifier input. Considering the two signal-source representations shown in Fig. 1.1, provide two sketches showing each signal-source representation connected to the input terminals (and corresponding input resistance) of a signal processor. What signal-processor input resistance will result in 90% of the open-circuit voltage being delivered to the processor? What input resistance will result in 90% of the short-circuit signal current entering the processor?

SECTION 1.2: FREQUENCY SPECTRUM OF SIGNALS

1.27 To familiarize yourself with typical values of angular frequency ω, conventional frequency f, and period T, complete the entries in the following table:

Case	ω (rad/s)	f (Hz)	T (s)
a		1×10^9	
b	1×10^9		
c			1×10^{-10}
d		60	
e	6.28×10^3		
f			1×10^{-6}

1.28 For the following peak or rms values of some important sine waves, calculate the corresponding other value:

(a) 117 V_{rms}, a household-power voltage in North America
(b) 33.9 V_{peak}, a somewhat common peak voltage in rectifier circuits
(c) 220 V_{rms}, a household-power voltage in parts of Europe
(d) 220 kV_{rms}, a high-voltage transmission-line voltage in North America

1.29 Give expressions for the sine-wave voltage signals having:

(a) 10-V peak amplitude and 10-kHz frequency
(b) 120-V rms and 60-Hz frequency
(c) 0.2-V peak-to-peak and 1000-rad/s frequency
(d) 100-mV peak and 1-ms period

1.30 Using the information provided by Eq. (1.2) in association with Fig. 1.4, characterize the signal represented by $v(t) = 1/2 + 2/\pi\,(\sin 2000\pi t + \frac{1}{3}\sin 6000\pi t + \frac{1}{5}\sin 10{,}000\pi t + \cdots)$. Sketch the waveform. What is its average value? Its peak-to-peak value? Its lowest value? Its highest value? Its frequency? Its period?

1.31 Measurements taken of a square-wave signal using a frequency-selective voltmeter (called a spectrum analyzer) show its spectrum to contain adjacent components (spectral lines) at 98 kHz and 126 kHz of amplitudes 63 mV and 49 mV, respectively. For this signal, what would direct measurement of the fundamental show its frequency and amplitude to be? What is the rms value of the fundamental? What are the peak-to-peak amplitude and period of the originating square wave?

1.32 What is the fundamental frequency of the highest-frequency square wave for which the fifth harmonic is barely audible by a relatively young listener? What is the fundamental frequency of the lowest-frequency square wave for which the fifth and some of the higher harmonics are directly heard? (Note that the psychoacoustic properties of human hearing allow a listener to sense the lower harmonics as well).

1.33 Find the amplitude of a symmetrical square wave of period T that provides the same power as a sine wave of peak amplitude $\hat{V}$ and the same frequency. Does this result depend on equality of the frequencies of the two waveforms?

SECTION 1.3: ANALOG AND DIGITAL SIGNALS

1.34 Give the binary representation of the following decimal numbers: 0, 5, 8, 25, and 57.

1.35 Consider a 4-bit digital word $b_3b_2b_1b_0$ in a format called signed-magnitude, in which the most-significant bit, b_3, is interpreted as a sign bit—0 for positive and 1 for negative values. List the values that can be represented by this scheme. What is peculiar about the representation of zero? For a particular analog-to-digital converter (ADC), each

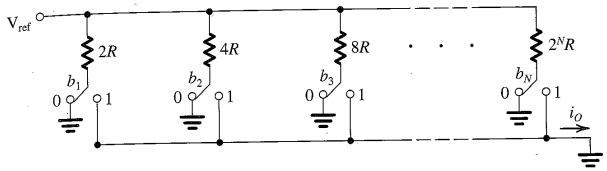


FIGURE P1.37

change in b_0 corresponds to a 0.5-V change in the analog input. What is the full range of the analog signal that can be represented? What signed-magnitude digital code results for an input of +2.5 V? For −3.0 V? For +2.7 V? For −2.8 V?

1.36 Consider an N-bit ADC whose analog input varies between 0 and V_{FS} (where the subscript FS denotes "full scale").

(a) Show that the least significant bit (LSB) corresponds to a change in the analog signal of $V_{FS}/(2^N - 1)$. This is the resolution of the converter.
(b) Convince yourself that the maximum error in the conversion (called the quantization error) is half the resolution; that is, the quantization error = $V_{FS}/2(2^N - 1)$.
(c) For $V_{FS} = 10$ V, how many bits are required to obtain a resolution of 5 mV or better? What is the actual resolution obtained? What is the resulting quantization error?

1.37 Figure P1.37 shows the circuit of an N-bit digital-to-analog converter (DAC). Each of the N bits of the digital word to be converted controls one of the switches. When the bit is 0, the switch is in the position labeled 0; when the bit is 1, the switch is in the position labeled 1. The analog output is the current i_O. V_{ref} is a constant reference voltage.

(a) Show that

$$i_O = \frac{V_{ref}}{R}\left(\frac{b_1}{2^1} + \frac{b_2}{2^2} + \cdots + \frac{b_N}{2^N}\right)$$

(b) Which bit is the LSB? Which is the MSB?
(c) For $V_{ref} = 10$ V, $R = 5$ kΩ, and $N = 6$, find the maximum value of i_O obtained. What is the change in i_O resulting from the LSB changing from 0 to 1?

1.38 In compact-disc (CD) audio technology, the audio signal is sampled at 44.1 kHz. Each sample is represented by 16 bits. What is the speed of this system in bits/second?

SECTION 1.4: AMPLIFIERS

1.39 Various amplifier and load combinations are measured as listed below using rms values. For each, find the voltage, current, and power gains (A_v, A_i, and A_p, respectively) both as ratios and in dB:

(a) $v_I = 100$ mV, $i_I = 100$ μA, $v_O = 10$ V, $R_L = 100$ Ω
(b) $v_I = 10$ μV, $i_I = 100$ nA, $v_O = 2$ V, $R_L = 10$ kΩ
(c) $v_I = 1$ V, $i_I = 1$ mA, $v_O = 10$ V, $R_L = 10$ Ω

1.40 An amplifier operating from ±3 V supplies provides a 2.2-V_{peak} sine wave across a 100-Ω load when provided with a 0.2-V_{peak} input from which 1.0 mA_{peak} is drawn. The average current in each supply is measured to be 20 mA. Find the voltage gain, current gain, and power gain expressed as ratios and in dB as well as the supply power, amplifier dissipation, and amplifier efficiency.

1.41 An amplifier using balanced power supplies is known to saturate for signals extending within 1.2 V of either supply. For linear operation, its gain is 500 V/V. What is the rms value of the largest undistorted sine-wave output available, and input needed, with ±5-V supplies? With ±10-V supplies? With ±15-V supplies?

1.42 Symmetrically saturating amplifiers, operating in the so-called clipping mode, can be used to convert sine waves to pseudo-square waves. For an amplifier with a small-signal gain of 1000 and clipping levels of ±9 V, what peak value of input sinusoid is needed to produce an output whose extremes are just at the edge of clipping? Clipped 90% of the time? Clipped 99% of the time?

1.43 A particular amplifier operating from a single supply exhibits clipped peaks for signals intended to extend above 8 V and below 1.5 V. What is the peak value of the largest possible undistorted sine wave when this amplifier is biased at 4 V? At what bias point is the largest undistorted sine wave available?

D*1.44 An amplifier designed using a single metal-oxide-semiconductor (MOS) transistor has the transfer characteristic

$$v_O = 10 - 5(v_I - 2)^2$$

where v_I and v_O are in volts. This transfer characteristic applies for $2 \le v_I \le v_O + 2$ and v_O positive. At the limits of this region the amplifier saturates.

(a) Sketch and clearly label the transfer characteristic. What are the saturation levels L_+ and L_- and the corresponding values of v_I?

(b) Bias the amplifier to obtain a dc output voltage of 5 V. What value of input dc voltage V_I is required?
(c) Calculate the value of the small-signal voltage gain at the bias point.
(d) If a sinusoidal input signal is superimposed on the dc bias voltage V_I, that is,

$$v_I = V_I + V_i \cos \omega t$$

find the resulting v_O. Using the trigonometric identity $\cos^2 \theta = \frac{1}{2} + \frac{1}{2} \cos 2\theta$, express v_O as the sum of a dc component, a signal component with frequency ω, and a sinusoidal component with frequency 2ω. The latter component is undesirable and is a result of the nonlinear transfer characteristic of the amplifier. If it is required to limit the ratio of the second-harmonic component to the fundamental component to 1% (this ratio is known as the second-harmonic distortion), what is the corresponding upper limit on V_i? What output amplitude results?

SECTION 1.5: CIRCUIT MODELS FOR AMPLIFIERS

1.45 Consider the voltage-amplifier circuit model shown in Fig. 1.17(b), in which $A_{vo} = 10$ V/V under the following conditions:

(a) $R_i = 10R_s$, $R_L = 10R_o$
(b) $R_i = R_s$, $R_L = R_o$
(c) $R_i = R_s/10$, $R_L = R_o/10$

Calculate the overall voltage gain v_o/v_s in each case, expressed both directly and in dB.

1.46 An amplifier with 40 dB of small-signal open-circuit voltage gain, an input resistance of 1 MΩ, and an output resistance of 10 Ω drives a load of 100 Ω. What voltage and power gains (expressed in dB) would you expect with the load connected? If the amplifier has a peak output-current limitation of 100 mA, what is the rms value of the largest sine-wave input for which an undistorted output is possible? What is the corresponding output power available?

1.47 A 10-mV signal source having an internal resistance of 100 kΩ is connected to an amplifier for which the input resistance is 10 kΩ, the open-circuit voltage gain is 1000 V/V, and the output resistance is 1 kΩ. The amplifier is connected in turn to a 100-Ω load. What overall voltage gain results as measured from the source internal voltage to the load? Where did all the gain go? What would the gain be if the source was connected directly to the load? What is the ratio of these two gains? This ratio is a useful measure of the benefit the amplifier brings.

1.48 A buffer amplifier with a gain of 1 V/V has an input resistance of 1 MΩ and an output resistance of 10 Ω. It is connected between a 1-V, 100-kΩ source and a 100-Ω load. What load voltage results? What are the corresponding voltage, current, and power gains expressed in dB?

1.49 Consider the cascade amplifier of Example 1.3. Find the overall voltage gain v_o/v_s obtained when the first and second stages are interchanged. Compare this value with the result in Example 1.3, and comment.

1.50 You are given two amplifiers, A and B, to connect in cascade between a 10-mV, 100-kΩ source and a 100-Ω load. The amplifiers have voltage gain, input resistance, and output resistance as follows: For A, 100 V/V, 10 kΩ, 10 kΩ, respectively; for B, 1 V/V, 100 kΩ, 100 kΩ, respectively. Your problem is to decide how the amplifiers should be connected. To proceed, evaluate the two possible connections between source S and load L, namely, SABL and SBAL. Find the voltage gain for each both as a ratio and in dB. Which amplifier arrangement is best?

D*1.51 A designer has available voltage amplifiers with an input resistance of 10 kΩ, an output resistance of 1 kΩ, and an open-circuit voltage gain of 10. The signal source has a 10 kΩ resistance and provides a 10-mV rms signal, and it is required to provide a signal of at least 2 V rms to a 1-kΩ load. How many amplifier stages are required? What is the output voltage actually obtained.

D*1.52 Design an amplifier that provides 0.5 W of signal power to a 100-Ω load resistance. The signal source provides a 30-mV rms signal and has a resistance of 0.5 MΩ. Three types of voltage amplifier stages are available:

(a) A high-input-resistance type with $R_i = 1$ MΩ, $A_{vo} = 10$, and $R_o = 10$ kΩ
(b) A high-gain type with $R_i = 10$ kΩ, $A_{vo} = 100$, and $R_o = 1$ kΩ
(c) A low-output-resistance type with $R_i = 10$ kΩ, $A_{vo} = 1$, and $R_o = 20$ Ω

Design a suitable amplifier using a combination of these stages. Your design should utilize the minimum number of stages and should ensure that the signal level is not reduced below 10 mV at any point in the amplifier chain. Find the load voltage and power output realized.

D*1.53 It is required to design a voltage amplifier to be driven from a signal source having a 10-mV peak amplitude and a source resistance of 10 kΩ to supply a peak output of 3 V across a 1-kΩ load.

(a) What is the required voltage gain from the source to the load?
(b) If the peak current available from the source is 0.1 μA, what is the smallest input resistance allowed? For the design with this value of R_i, find the overall current gain and power gain.

(c) If the amplifier power supply limits the peak value of the output open-circuit voltage to 5 V, what is the largest output resistance allowed?
(d) For the design with R_i as in (b) and R_o as in (c), what is the required value of open-circuit voltage gain $\left(\text{i.e., } \left.\frac{v_o}{v_i}\right|_{R_L=\infty}\right)$ of the amplifier?

(e) If, as a possible design option, you are able to increase R_i to the nearest value of the form 1×10^n Ω and to decrease R_o to the nearest value of the form 1×10^m Ω, find (i) the input resistance achievable; (ii) the output resistance achievable; and (iii) the open-circuit voltage gain now required to meet the specifications.

D1.54 A voltage amplifier with an input resistance of 10 kΩ, an output resistance of 200 Ω, and a gain of 1000 V/V is connected between a 100-kΩ source with an open-circuit voltage of 10 mV and a 100-Ω load. For this situation:

(a) What output voltage results?
(b) What is the voltage gain from source to load?
(c) What is the voltage gain from the amplifier input to the load?
(d) If the output voltage across the load is twice that needed and there are signs of internal amplifier overload, suggest the location and value of a single resistor that would produce the desired output. Choose an arrangement that would cause minimum disruption to an operating circuit. (*Hint:* Use parallel rather than series connections.)

1.55 A current amplifier for which $R_i = 1$ kΩ, $R_o = 10$ kΩ, and $A_{is} = 100$ A/A is to be connected between a 100-mV source with a resistance of 100 kΩ and a load of 1 kΩ. What are the values of current gain i_o/i_i, of voltage gain v_o/v_s, and of power gain expressed directly and in dB?

1.56 A transconductance amplifier with $R_i = 2$ kΩ, $G_m = 40$ mA/V, and $R_o = 20$ kΩ is fed with a voltage source having a source resistance of 2 kΩ and is loaded with a 1-kΩ resistance. Find the voltage gain realized.

D1.57** A designer is required to provide, across a 10-kΩ load, the weighted sum, $v_O = 10v_1 + 20v_2$, of input signals v_1 and v_2, each having a source resistance of 10 kΩ. She has a number of transconductance amplifiers for which the input and output resistances are both 10 kΩ and $G_m = 20$ mA/V, together with a selection of suitable resistors. Sketch an appropriate amplifier topology with additional resistors selected to provide the desired result. (*Hint:* In your design, arrange to add currents.)

1.58 Figure P1.58 shows a transconductance amplifier whose output is *fed back* to its input. Find the input resistance R_{in} of the resulting one-port network. (*Hint:* Apply a test voltage v_x between the two input terminals, and find the current i_x drawn from the source. Then, $R_{in} \equiv v_x/i_x$.)

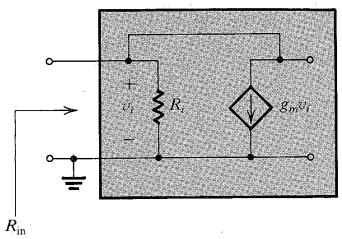


FIGURE P1.58

D1.59 It is required to design an amplifier to sense the open-circuit output voltage of a transducer and to provide a proportional voltage across a load resistor. The equivalent source resistance of the transducer is specified to vary in the range of 1 kΩ to 10 kΩ. Also, the load resistance varies in the range of 1 kΩ to 10 kΩ. The change in load voltage corresponding to the specified change in R_s should be 10% at most. Similarly, the change in load voltage corresponding to the specified change in R_L should be limited to 10%. Also, corresponding to a 10-mV transducer open-circuit output voltage, the amplifier should provide a minimum of 1 V across the load. What type of amplifier is required? Sketch its circuit model, and specify the values of its parameters. Specify appropriate values for R_i and R_o of the form 1×10^m Ω.

D1.60 It is required to design an amplifier to sense the short-circuit output current of a transducer and to provide a proportional current through a load resistor. The equivalent source resistance of the transducer is specified to vary in the range of 1 kΩ to 10 kΩ. Similarly, the load resistance is known to vary over the range of 1 kΩ to 10 kΩ. The change in load current corresponding to the specified change in R_s is required to be limited to 10%. Similarly, the change in load current corresponding to the specified change in R_L should be 10% at most. Also, for a nominal short-circuit output current of the transducer of 10 μA, the amplifier is required to provide a minimum of 1 mA through the load. What type of amplifier is required? Sketch the circuit model of the amplifier, and specify values for its parameters. Select appropriate values for R_i and R_o in the form 1×10^m Ω.

D1.61 It is required to design an amplifier to sense the open-circuit output voltage of a transducer and to provide a proportional current through a load resistor. The equivalent source resistance of the transducer is specified to vary in the range of 1 kΩ to 10 kΩ. Also, the load resistance is known to

vary in the range of 1 kΩ to 10 kΩ. The change in the current supplied to the load corresponding to the specified change in R_s is to be 10% at most. Similarly, the change in load current corresponding to the specified change in R_L is to be 10% at most. Also, for a nominal transducer open-circuit output voltage of 10 mV, the amplifier is required to provide a minimum of 1 mA current through the load. What type of amplifier is required? Sketch the amplifier circuit model, and specify values for its parameters. For R_i and R_o, specify values in the form 1×10^m Ω.

D1.62 It is required to design an amplifier to sense the short-circuit output current of a transducer and to provide a proportional voltage across a load resistor. The equivalent source resistance of the transducer is specified to vary in the range of 1 kΩ to 10 kΩ. Similarly, the load resistance is known to vary in the range of 1 kΩ to 10 kΩ. The change in load voltage corresponding to the specified change in R_s should be 10% at most. Similarly, the change in load voltage corresponding to the specified change in R_L is to be limited to 10%. Also, for a nominal transducer short-circuit output current of 10 μA, the amplifier is required to provide a minimum voltage across the load of 1 V. What type of amplifier is required? Sketch its circuit model, and specify the values of the model parameters. For R_i and R_o, specify appropriate values in the form 1×10^m Ω.

1.63 For the circuit in Fig. P1.63, show that

$$\frac{v_c}{v_b} = \frac{-\beta R_L}{r_\pi + (\beta+1)R_E}$$

and

$$\frac{v_e}{v_b} = \frac{R_E}{R_E + [r_\pi/(\beta+1)]}$$

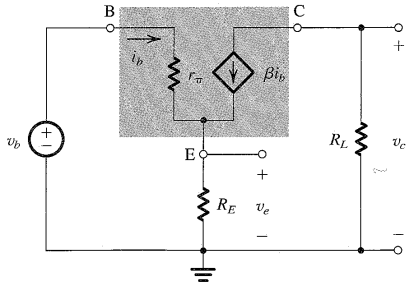
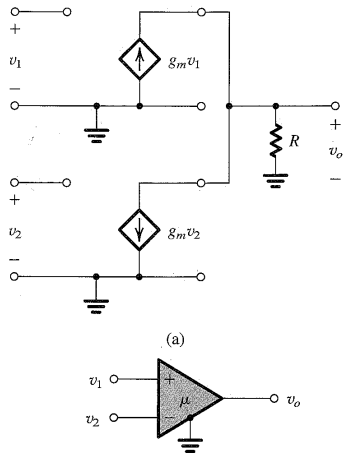


FIGURE P1.63

1.64 An amplifier with an input resistance of 10 kΩ, when driven by a current source of 1 μA and a source resistance of 100 kΩ, has a short-circuit output current of 10 mA and an open-circuit output voltage of 10 V. When driving a 4-kΩ load, what are the values of the voltage gain, current gain, and power gain expressed as ratios and in dB?

1.65 Figure P1.65(a) shows two transconductance amplifiers connected in a special configuration. Find v_o in terms of v_1 and v_2. Let $g_m = 100$ mA/V and $R = 5$ kΩ. If $v_1 = v_2 = 1$ V, find the value of v_o. Also, find v_o for the case $v_1 = 1.01$ V and $v_2 = 0.99$ V. (*Note:* This circuit is called a **differential amplifier** and is given the symbol shown in Fig. P1.65(b). A particular type of differential amplifier known as an **operational amplifier** will be studied in Chapter 2.)



(a)

(b)

FIGURE P1.65

SECTION 1.6: FREQUENCY RESPONSE OF AMPLIFIERS

1.66 Using the voltage-divider rule, derive the transfer functions $T(s) \equiv V_o(s)/V_i(s)$ of the circuits shown in Fig. 1.22, and show that the transfer functions are of the form given at the top of Table 1.2.

1.67 Figure P1.67 shows a signal source connected to the input of an amplifier. Here R_s is the source resistance, and R_i and C_i are the input resistance and input capacitance, respectively, of the amplifier. Derive an expression for $V_i(s)/V_s(s)$, and show that it is of the low-pass STC type. Find the 3-dB frequency for the case $R_s = 20$ kΩ, $R_i = 80$ kΩ, and $C_i = 5$ pF.

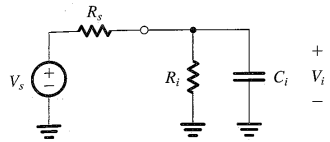


FIGURE P1.67

1.68 For the circuit shown in Fig. P1.68, find the transfer function $T(s) = V_o(s)/V_i(s)$, and arrange it in the appropriate standard form from Table 1.2. Is this a high-pass or a low-pass network? What is its transmission at very high frequencies? [Estimate this directly, as well as by letting $s \to \infty$ in your expression for $T(s)$.] What is the corner frequency ω_0? For $R_1 = 10$ kΩ, $R_2 = 40$ kΩ, and $C = 0.1$ μF, find f_0. What is the value of $|T(j\omega_0)|$?

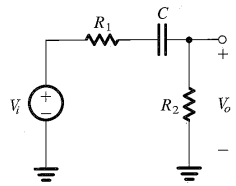


FIGURE P1.68

D1.69 It is required to couple a voltage source V_s with a resistance R_s to a load R_L via a capacitor C. Derive an expression for the transfer function from source to load (i.e., V_L/V_s), and show that it is of the high-pass STC type. For $R_s = 5$ kΩ and $R_L = 20$ kΩ, find the smallest coupling capacitor that will result in a 3-dB frequency no greater than 10 Hz.

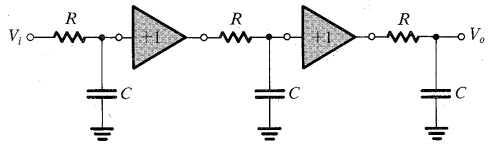


FIGURE P1.72

1.70 Measurement of the frequency response of an amplifier yields the data in the following table:

f (Hz)	$\lvert T\rvert$ (dB)	$\angle T$ (°)
0	40	0
100	40	0
1000		
10^4	37	−45
10^5	20	
	0	

Provide plausible approximate values for the missing entries. Also, sketch and clearly label the magnitude frequency response (i.e., provide a Bode plot) for this amplifier.

1.71 Measurement of the frequency response of an amplifier yields the data in the following table:

f (Hz)		10	10^2	10^3	10^4	10^5	10^6	10^7	
$\lvert T\rvert$ (dB)	0	20	37	40			37	20	0

Provide approximate plausible values for the missing table entries. Also, sketch and clearly label the magnitude frequency response (Bode plot) of this amplifier.

1.72 The unity-gain voltage amplifiers in the circuit of Fig. P1.72 have infinite input resistances and zero output resistances and thus function as perfect buffers. Convince yourself that the overall gain V_o/V_i will drop by 3 dB below the value at dc at the frequency for which the gain of each RC circuit is 1.0 dB down. What is that frequency in terms of CR?

1.73 An internal node of a high-frequency amplifier whose Thévenin-equivalent node resistance is 100 kΩ is accidentally shunted to ground by a capacitor (i.e., the node is connected to ground through a capacitor) through a manufacturing error. If the measured 3 dB bandwidth of the amplifier is reduced from the expected 6 MHz to 120 kHz, estimate the value of the shunting capacitor. If the original cutoff frequency can be attributed to a small parasitic capacitor at the same internal node (i.e., between the node and ground), what would you estimate it to be?

D*1.74 A designer wishing to lower the overall upper 3-dB frequency of a three-stage amplifier to 10 kHz considers shunting one of two nodes: Node A, between the output of the first stage and the input of the second stage, and Node B, between the output of the second stage and the input of the third stage, to ground with a small capacitor. While measuring the overall frequency response of the amplifier, she shunts a capacitor of 1 nF, first to node A and then to node B, lowering the 3-dB frequency from 2 MHz to 150 kHz and 15 kHz, respectively. If she knows that each amplifier stage has an input resistance of 100 kΩ, what output resistance must the driving stage have at node A? At node B? What capacitor value should she connect to which node to solve her design problem most economically?

D1.75 An amplifier with an input resistance of 100 kΩ and an output resistance of 1 kΩ is to be capacitor-coupled to a 10-kΩ source and a 1-kΩ load. Available capacitors have values only of the form 1×10^{-n} F. What are the values of the smallest capacitors needed to ensure that the corner frequency associated with each is less than 100 Hz? What actual corner frequencies result? For the situation in which the basic amplifier has an open-circuit voltage gain (A_{vo}) of 100 V/V, find an expression for $T(s) = V_o(s)/V_s(s)$.

***1.76** A voltage amplifier has the transfer function

$$A_v = \frac{100}{\left(1 + j\frac{f}{10^4}\right)\left(1 + \frac{10^2}{jf}\right)}$$

Using the Bode plots for low-pass and high-pass STC networks (Figs. 1.23 and 1.24), sketch a Bode plot for $|A_v|$. Give approximate values for the gain magnitude at $f = 10$ Hz, 10^2 Hz, 10^3 Hz, 10^4 Hz, 10^5 Hz, 10^6 Hz, and 10^7 Hz. Find the bandwidth of the amplifier (defined as the frequency range over which the gain remains within 3 dB of the maximum value).

***1.77** For the circuit shown in Fig. P1.77 first, evaluate $T_i(s) = V_i(s)/V_s(s)$ and the corresponding cutoff (corner) frequency. Second, evaluate $T_o(s) = V_o(s)/V_i(s)$ and the corresponding cutoff frequency. Put each of the transfer functions in the standard form (see Table 1.2), and combine them to form the overall transfer function, $T(s) = T_i(s) \times T_o(s)$. Provide a Bode magnitude plot for $|T(j\omega)|$. What is the bandwidth between 3-dB cutoff points?

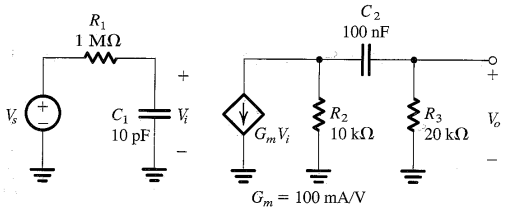


FIGURE P1.77

D1.78** A transconductance amplifier having the equivalent circuit shown in Table 1.1 is fed with a voltage source V_s having a source resistance R_s, and its output is connected to a load consisting of a resistance R_L in parallel with a capacitance C_L. For given values of R_s, R_L, and C_L, it is required to specify the values of the amplifier parameters R_i, G_m, and R_o to meet the following design constraints:

(a) At most, x% of the input signal is lost in coupling the signal source to the amplifier (i.e., $V_i \geq [1 - (x/100)]V_s$).
(b) The 3-dB frequency of the amplifier is equal to or greater than a specified value $f_{3\,\text{dB}}$.
(c) The dc gain V_o/V_s is equal to or greater than a specified value A_0.

Show that these constraints can be met by selecting

$$R_i \geq \left(\frac{100}{x} - 1\right)R_s$$

$$R_o \leq \frac{1}{2\pi f_{3\,\text{dB}} C_L - (1/R_L)}$$

$$G_m \geq \frac{A_0/[1 - (x/100)]}{(R_L \parallel R_o)}$$

Find R_i, R_o, and G_m for $R_s = 10$ kΩ, $x = 20\%$, $A_0 = 80$, $R_L = 10$ kΩ, $C_L = 10$ pF, and $f_{3\,\text{dB}} = 3$ MHz.

***1.79** Use the voltage-divider rule to find the transfer function $V_o(s)/V_i(s)$ of the circuit in Fig. P1.79. Show that the transfer function can be made independent of frequency if the condition $C_1R_1 = C_2R_2$ applies. Under this condition the circuit is called a **compensated attenuator** and is frequently employed in the design of oscilloscope probes. Find the transmission of the compensated attenuator in terms of R_1 and R_2.

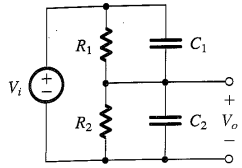


FIGURE P1.79

***1.80** An amplifier with a frequency response of the type shown in Fig. 1.21 is specified to have a phase shift of magnitude no greater than 11.4° over the amplifier bandwidth, which extends from 100 Hz to 1 kHz. It has been found that the gain falloff at the low-frequency end is determined by the response of a high-pass STC circuit and that at the high-frequency end it is determined by a low-pass STC circuit. What do you expect the corner frequencies of these two circuits to be? What is the drop in gain in decibels (relative to the maximum gain) at the two frequencies that define the amplifier bandwidth? What are the frequencies at which the drop in gain is 3 dB?

SECTION 1.7: DIGITAL LOGIC INVERTERS

1.81 A particular logic inverter is specified to have $V_{IL} = 1.3$ V, $V_{IH} = 1.7$ V, $V_{OL} = 0$ V, and $V_{OH} = 3.3$ V. Find the high and low noise margins, NM_H and NM_L.

1.82 The voltage-transfer characteristic of a particular logic inverter is modeled by three straight-line segments in the manner shown in Fig. 1.29. If $V_{IL} = 1.5$ V, $V_{IH} = 2.5$ V, $V_{OL} = 0.5$ V, and $V_{OH} = 4$ V, find:

(a) The noise margins
(b) The value of v_I at which $v_O = v_I$ (known as the **inverter threshold**)
(c) The voltage gain in the transition region

1.83 For a particular inverter design using a power supply V_{DD}, $V_{OL} = 0.1V_{DD}$, $V_{OH} = 0.8V_{DD}$, $V_{IL} = 0.4V_{DD}$, and $V_{IH} = 0.6V_{DD}$. What are the noise margins? What is the width of the transition region? For a minimum noise margin of 1 V, what value of V_{DD} is required?

1.84 A logic circuit family that used to be very popular is Transistor-Transistor Logic (TTL). The TTL logic gates and other building blocks are available commercially in small-scale integrated (SSI) and medium-scale-integrated (MSI) packages. Such packages can be assembled on printed-circuit boards to implement a digital system. The device data sheets provide the following specifications of the basic TTL inverter (of the SN7400 type):

Logic-1 input level required to ensure a logic-0 level at the output: MIN (minimum) 2 V
Logic-0 input level required to ensure a logic-1 level at the output: MAX (maximum) 0.8 V
Logic-1 output voltage: MIN 2.4 V, TYP (typical) 3.3 V
Logic-0 output voltage: TYP 0.22 V, MAX 0.4 V
Logic-0-level supply current: TYP 3 mA, MAX 5 mA
Logic-1-level supply current: TYP 1 mA, MAX 2 mA
Propagation delay time to logic-0 level (t_{PHL}): TYP 7 ns, MAX 15 ns
Propagation delay time to logic-1 level (t_{PLH}): TYP 11 ns, MAX 22 ns

(a) Find the worst-case values of the noise margins.
(b) Assuming that the inverter is in the 1-state 50% of the time and in the 0-state 50% of the time, find the average static power dissipation in a typical circuit. The power supply is 5 V.
(c) Assuming that the inverter drives a capacitance $C_L = 45$ pF and is switched at a 1-MHz rate, use the formula in Eq. (1.28) to estimate the dynamic power dissipation.
(d) Find the propagation delay t_P.

1.85 Consider an inverter implemented as in Fig. 1.31(a). Let $V_{DD} = 5$ V, $R = 2$ kΩ, $V_{\text{offset}} = 0.1$ V, $R_{\text{on}} = 200$ Ω, $V_{IL} = 1$ V, and $V_{IH} = 2$ V.

(a) Find V_{OL}, V_{OH}, NM_H, and NM_L.
(b) The inverter is driving N identical inverters. Each of these load inverters, or **fan-out** inverters as they are usually called, is specified to require an input current of 0.2 mA when the input voltage (of the fan-out inverter) is high and zero current when the input voltage is low. Noting that the input currents of the fan-out inverters will have to be supplied through R of the driving inverter, find the resulting value of V_{OH} and of NM_H as a function of the number of fan-out inverters N. Hence find the maximum value N can have while the inverter is still providing an NM_H value at least equal to its NM_L.
(c) Find the static power dissipation in the inverter in the two cases: (i) the output is low, and (ii) the output is high and driving the maximum fan-out found in (b).

1.86 A logic inverter is implemented using the arrangement of Fig. 1.32 with switches having $R_{\text{on}} = 1$ kΩ, $V_{DD} = 5$ V, and $V_{IL} = V_{IH} = V_{DD}/2$.

(a) Find V_{OL}, V_{OH}, NM_L, and NM_H.
(b) If v_I rises instantaneously from 0 V to +5 V and assuming the switches operate instantaneously—that is, at $t = 0$, PU opens, and PD closes—find an expression for $v_O(t)$ assuming that a capacitance C is connected between the output node and ground. Hence find the high-to-low propagation delay (t_{PHL}) for $C = 1$ pF. Also find t_{THL} (see Fig. 1.35).

(c) Repeat (b) for v_I falling instantaneously from +5 V to 0 V. Again assume that PD opens and PU closes instantaneously. Find an expression for $v_O(t)$, and hence find t_{PLH} and t_{TLH}.

1.87 For the current-mode inverter shown in Fig. 1.33, let $V_{CC} = 5$ V, $I_{EE} = 1$ mA, and $R_{C1} = R_{C2} = 2$ kΩ. Find V_{OL} and V_{OH}.

1.88 Consider a logic inverter of the type shown in Fig. 1.32. Let $V_{DD} = 5$ V, and let a 10-pF capacitance be connected between the output node and ground. If the inverter is switched at the rate of 100 MHz, use the expression in Eq. (1.28) to estimate the dynamic power dissipation. What is the average current drawn from the dc power supply?

D1.89** We wish to investigate the design of the inverter shown in Fig. 1.31(a). In particular we wish to determine the value for R. Selection of a suitable value for R is determined by two considerations: propagation delay, and power dissipation.

(a) Show that if v_I changes instantaneously from high to low and assuming that the switch opens instantaneously, the output voltage obtained across a load capacitance C will be

$$v_O(t) = V_{OH} - (V_{OH} - V_{OL})e^{-t/\tau_1}$$

where $\tau_1 = CR$. Hence show that the time required for $v_O(t)$ to reach the 50% point, $\frac{1}{2}(V_{OH} + V_{OL})$, is

$$t_{PLH} = 0.69CR$$

(b) Following a steady state, if v_I goes high and assuming that the switch closes immediately and has the equivalent circuit in Fig. 1.31, show that the output falls exponentially according to

$$v_O(t) = V_{OL} + (V_{OH} - V_{OL})e^{-t/\tau_2}$$

where $\tau_2 = C(R \parallel R_{on}) \cong CR_{on}$ for $R_{on} \ll R$. Hence show that the time for $v_O(t)$ to reach the 50% point is

$$t_{PHL} = 0.69CR_{on}$$

(c) Use the results of (a) and (b) to obtain the inverter propagation delay, defined as the average of t_{PLH} and t_{PHL} as

$$\tau_P \cong 0.35CR \text{ for } R_{on} \ll R$$

(d) Assuming that V_{offset} of the switch is much smaller than V_{DD}, show that for an inverter that spends half the time in the 0 state and half the time in the 1 state, the average static power dissipation is

$$P = \frac{1}{2}\frac{V_{DD}^2}{R}$$

(e) Now that the trade-offs in selecting R should be obvious, show that, for $V_{DD} = 5$ V and $C = 10$ pF, to obtain a propagation delay no greater than 10 ns and a power dissipation no greater than 10 mW, R should be in a specific range. Find that range and select an appropriate value for R. Then determine the resulting values of t_P and P.

CHAPTER 2

Operational Amplifiers

INTRODUCTION

Having learned basic amplifier concepts and terminology, we are now ready to undertake the study of a circuit building block of universal importance: the operational amplifier (op amp). Op amps have been in use for a long time, their initial applications being primarily in the areas of analog computation and sophisticated instrumentation. Early op amps were constructed from discrete components (vacuum tubes and then transistors, and resistors), and their cost was prohibitively high (tens of dollars). In the mid-1960s the first integrated-circuit (IC) op amp was produced. This unit (the μA 709) was made up of a relatively large number of transistors and resistors all on the same silicon chip. Although its characteristics were poor (by today's standards) and its price was still quite high, its appearance signaled a new era in electronic circuit design. Electronics engineers started using op amps in large quantities, which caused their price to drop dramatically. They also demanded better-quality op amps. Semiconductor manufacturers responded quickly, and within the span of a few years, high-quality op amps became available at extremely low prices (tens of cents) from a large number of suppliers.

One of the reasons for the popularity of the op amp is its versatility. As we will shortly see, one can do almost anything with op amps! Equally important is the fact that the IC op amp has characteristics that closely approach the assumed ideal. This implies that it is quite