D*1.74 A designer wishing to lower the overall upper 3-dB frequency of a three-stage amplifier to 10 kHz considers shunting one of two nodes: Node A, between the output of the first stage and the input of the second stage, and Node B, between the output of the second stage and the input of the third stage, to ground with a small capacitor. While measuring the overall frequency response of the amplifier, she shunts a capacitor of 1 nF, first to node A and then to node B, lowering the 3-dB frequency from 2 MHz to 150 kHz and 15 kHz, respectively. If she knows that each amplifier stage has an input resistance of 100 kΩ, what output resistance must the driving stage have at node A? At node B? What capacitor value should she connect to which node to solve her design problem most economically?

D1.75 An amplifier with an input resistance of 100 kΩ and an output resistance of 1 kΩ is to be capacitor-coupled to a 10-kΩ source and a 1-kΩ load. Available capacitors have values only of the form 1×10^{-n} F. What are the values of the smallest capacitors needed to ensure that the corner frequency associated with each is less than 100 Hz? What actual corner frequencies result? For the situation in which the basic amplifier has an open-circuit voltage gain (A_{vo}) of 100 V/V, find an expression for $T(s) = V_o(s)/V_s(s)$.

***1.76** A voltage amplifier has the transfer function

$$A_v = \frac{100}{\left(1+j\frac{f}{10^4}\right)\left(1+\frac{10^2}{jf}\right)}$$

Using the Bode plots for low-pass and high-pass STC networks (Figs. 1.23 and 1.24), sketch a Bode plot for $|A_v|$. Give approximate values for the gain magnitude at $f = 10$ Hz, 10^2 Hz, 10^3 Hz, 10^4 Hz, 10^5 Hz, 10^6 Hz, and 10^7 Hz. Find the bandwidth of the amplifier (defined as the frequency range over which the gain remains within 3 dB of the maximum value).

***1.77** For the circuit shown in Fig. P1.77 first, evaluate $T_i(s) = V_i(s)/V_s(s)$ and the corresponding cutoff (corner) frequency. Second, evaluate $T_o(s) = V_o(s)/V_i(s)$ and the corresponding cutoff frequency. Put each of the transfer functions in the standard form (see Table 1.2), and combine them to form the overall transfer function, $T(s) = T_i(s) \times T_o(s)$. Provide a Bode magnitude plot for $|T(j\omega)|$. What is the bandwidth between 3-dB cutoff points?

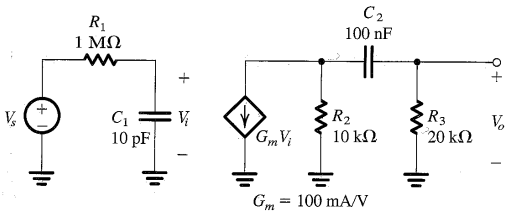

FIGURE P1.77

D1.78** A transconductance amplifier having the equivalent circuit shown in Table 1.1 is fed with a voltage source V_s having a source resistance R_s, and its output is connected to a load consisting of a resistance R_L in parallel with a capacitance C_L. For given values of R_s, R_L, and C_L, it is required to specify the values of the amplifier parameters R_i, G_m, and R_o to meet the following design constraints:

(a) At most, x% of the input signal is lost in coupling the signal source to the amplifier (i.e., $V_i \geq [1-(x/100)]V_s$).
(b) The 3-dB frequency of the amplifier is equal to or greater than a specified value $f_{3\,\text{dB}}$.
(c) The dc gain V_o/V_s is equal to or greater than a specified value A_0.

Show that these constraints can be met by selecting

$$R_i \geq \left(\frac{100}{x}-1\right)R_s$$

$$R_o \leq \frac{1}{2\pi f_{3\,\text{dB}} C_L - (1/R_L)}$$

$$G_m \geq \frac{A_0/[1-(x/100)]}{(R_L \parallel R_o)}$$

Find R_i, R_o, and G_m for $R_s = 10$ kΩ, $x = 20\%$, $A_0 = 80$, $R_L = 10$ kΩ, $C_L = 10$ pF, and $f_{3\,\text{dB}} = 3$ MHz.

***1.79** Use the voltage-divider rule to find the transfer function $V_o(s)/V_i(s)$ of the circuit in Fig. P1.79. Show that the transfer function can be made independent of frequency if the condition $C_1R_1 = C_2R_2$ applies. Under this condition the circuit is called a **compensated attenuator** and is frequently employed in the design of oscilloscope probes. Find the transmission of the compensated attenuator in terms of R_1 and R_2.

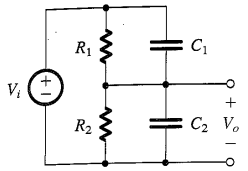

FIGURE P1.79

***1.80** An amplifier with a frequency response of the type shown in Fig. 1.21 is specified to have a phase shift of magnitude no greater than 11.4° over the amplifier bandwidth, which extends from 100 Hz to 1 kHz. It has been found that the gain falloff at the low-frequency end is determined by the response of a high-pass STC circuit and that at the high-frequency end it is determined by a low-pass STC circuit. What do you expect the corner frequencies of these two circuits to be? What is the drop in gain in decibels (relative to the maximum gain) at the two frequencies that define the amplifier bandwidth? What are the frequencies at which the drop in gain is 3 dB?

SECTION 1.7: DIGITAL LOGIC INVERTERS

1.81 A particular logic inverter is specified to have $V_{IL} = 1.3$ V, $V_{IH} = 1.7$ V, $V_{OL} = 0$ V, and $V_{OH} = 3.3$ V. Find the high and low noise margins, NM_H and NM_L.

1.82 The voltage-transfer characteristic of a particular logic inverter is modeled by three straight-line segments in the manner shown in Fig. 1.29. If $V_{IL} = 1.5$ V, $V_{IH} = 2.5$ V, $V_{OL} = 0.5$ V, and $V_{OH} = 4$ V, find:

(a) The noise margins
(b) The value of v_I at which $v_O = v_I$ (known as the **inverter threshold**)
(c) The voltage gain in the transition region

1.83 For a particular inverter design using a power supply V_{DD}, $V_{OL} = 0.1V_{DD}$, $V_{OH} = 0.8V_{DD}$, $V_{IL} = 0.4V_{DD}$, and $V_{IH} = 0.6V_{DD}$. What are the noise margins? What is the width of the transition region? For a minimum noise margin of 1 V, what value of V_{DD} is required?

1.84 A logic circuit family that used to be very popular is Transistor-Transistor Logic (TTL). The TTL logic gates and other building blocks are available commercially in small-scale integrated (SSI) and medium-scale-integrated (MSI) packages. Such packages can be assembled on printed-circuit boards to implement a digital system. The device data sheets provide the following specifications of the basic TTL inverter (of the SN7400 type):

Logic-1 input level required to ensure a logic-0 level at the output: MIN (minimum) 2 V
Logic-0 input level required to ensure a logic-1 level at the output: MAX (maximum) 0.8 V
Logic-1 output voltage: MIN 2.4 V, TYP (typical) 3.3 V
Logic-0 output voltage: TYP 0.22 V, MAX 0.4 V
Logic-0-level supply current: TYP 3 mA, MAX 5 mA
Logic-1-level supply current: TYP 1 mA, MAX 2 mA
Propagation delay time to logic-0 level (t_{PHL}): TYP 7 ns, MAX 15 ns
Propagation delay time to logic-1 level (t_{PLH}): TYP 11 ns, MAX 22 ns

(a) Find the worst-case values of the noise margins.
(b) Assuming that the inverter is in the 1-state 50% of the time and in the 0-state 50% of the time, find the average static power dissipation in a typical circuit. The power supply is 5 V.
(c) Assuming that the inverter drives a capacitance $C_L = 45$ pF and is switched at a 1-MHz rate, use the formula in Eq. (1.28) to estimate the dynamic power dissipation.
(d) Find the propagation delay t_P.

1.85 Consider an inverter implemented as in Fig. 1.31(a). Let $V_{DD} = 5$ V, $R = 2$ kΩ, $V_{\text{offset}} = 0.1$ V, $R_{\text{on}} = 200$ Ω, $V_{IL} = 1$ V, and $V_{IH} = 2$ V.

(a) Find V_{OL}, V_{OH}, NM_H, and NM_L.
(b) The inverter is driving N identical inverters. Each of these load inverters, or **fan-out** inverters as they are usually called, is specified to require an input current of 0.2 mA when the input voltage (of the fan-out inverter) is high and zero current when the input voltage is low. Noting that the input currents of the fan-out inverters will have to be supplied through R of the driving inverter, find the resulting value of V_{OH} and of NM_H as a function of the number of fan-out inverters N. Hence find the maximum value N can have while the inverter is still providing an NM_H value at least equal to its NM_L.
(c) Find the static power dissipation in the inverter in the two cases: (i) the output is low, and (ii) the output is high and driving the maximum fan-out found in (b).

1.86 A logic inverter is implemented using the arrangement of Fig. 1.32 with switches having $R_{\text{on}} = 1$ kΩ, $V_{DD} = 5$ V, and $V_{IL} = V_{IH} = V_{DD}/2$.

(a) Find V_{OL}, V_{OH}, NM_L, and NM_H.
(b) If v_I rises instantaneously from 0 V to +5 V and assuming the switches operate instantaneously—that is, at $t = 0$, PU opens, and PD closes—find an expression for $v_O(t)$ assuming that a capacitance C is connected between the output node and ground. Hence find the high-to-low propagation delay (t_{PHL}) for $C = 1$ pF. Also find t_{THL} (see Fig. 1.35).

−2.000 V and that at the negative input to be −3.000 V. For the amplifier to be ideal, what would you expect the voltage at the positive input to be? If the measured voltage at the positive input is −3.020 V, what is likely to be the actual gain of the amplifier?

2.4 A set of experiments are run on an op amp that is ideal except for having a finite gain A. The results are tabulated below. Are the results consistent? If not, are they reasonable, in view of the possibility of experimental error? What do they show the gain to be? Using this value, predict values of the measurements that were accidentally omitted (the blank entries).

Experiment #	v_1	v_2	v_o
1	0.00	0.00	0.00
2	1.00	1.00	0.00
3		1.00	1.00
4	1.00	1.10	10.1
5	2.01	2.00	−0.99
6	1.99	2.00	1.00
7	5.10		−5.10

2.5 Refer to Exercise 2.3. This problem explores an alternative internal structure for the op amp. In particular, we wish to model the internal structure of a particular op amp using two transconductance amplifiers and one transresistance amplifier. Suggest an appropriate topology. For equal transconductances G_m and a transresistance R_m, find an expression for the open-loop gain A. For $G_m = 100$ mA/V and $R_m = 10^6\ \Omega$, what value of A results?

2.6 The two wires leading from the output terminals of a transducer pick up an interference signal that is a 60-Hz, 1-V sinusoid. The output signal of the transducer is sinusoidal of 10-mV amplitude and 1000-Hz frequency. Give expressions for v_{cm}, v_d, and the total signal between each wire and the system ground.

2.7 Nonideal (i.e., real) operational amplifiers respond to both the differential and common-mode components of their input signals (refer to Fig. 2.4 for signal representation). Thus the output voltage of the op amp can be expressed as

$$v_O = A_d v_{Id} + A_{cm} v_{Icm}$$

where A_d is the differential gain (referred to simply as A in the text) and A_{cm} is the common-mode gain (assumed to be zero in the text). The op amp's effectiveness in rejecting common-mode signals is measured by its CMRR, defined as

$$\text{CMRR} = 20 \log \left| \frac{A_d}{A_{cm}} \right|$$

Consider an op amp whose internal structure is of the type shown in Fig. E2.3 except for a mismatch ΔG_m between the transconductances of the two channels; that is,

$$G_{m1} = G_m - \tfrac{1}{2}\Delta G_m$$

$$G_{m2} = G_m + \tfrac{1}{2}\Delta G_m$$

Find expressions for A_d, A_{cm}, and CMRR. If A_d is 80 dB and the two transconductances are matched to within 0.1% of each other, calculate A_{cm} and CMRR.

SECTION 2.2: THE INVERTING CONFIGURATION

2.8 Assuming ideal op amps, find the voltage gain v_o/v_i and input resistance R_{in} of each of the circuits in Fig. P2.8.

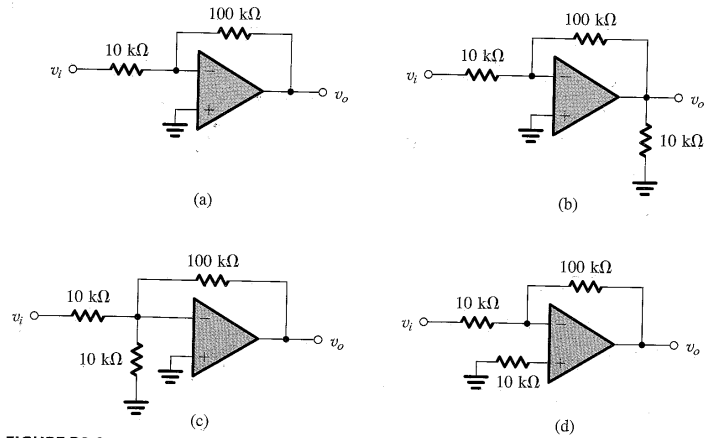

FIGURE P2.8

2.9 A particular inverting circuit uses an ideal op amp and two 10-kΩ resistors. What closed-loop gain would you expect? If a dc voltage of +5.00 V is applied at the input, what output result? If the 10-kΩ resistors are said to be "5% resistors," having values somewhere in the range (1 ± 0.05) times the nominal value, what range of outputs would you expect to actually measure for an input of precisely 5.00 V?

2.10 You are provided with an ideal op amp and three 10-kΩ resistors. Using series and parallel resistor combinations, how many different inverting-amplifier circuit topologies are possible? What is the largest (noninfinite) available voltage gain? What is the smallest (nonzero) available gain? What are the input resistances in these two cases?

2.11 For ideal op amps operating with the following feedback networks in the inverting configuration, what closed-loop gain results?

(a) $R_1 = 10$ kΩ, $R_2 = 10$ kΩ
(b) $R_1 = 10$ kΩ, $R_2 = 100$ kΩ
(c) $R_1 = 10$ kΩ, $R_2 = 1$ kΩ
(d) $R_1 = 100$ kΩ, $R_2 = 10$ MΩ
(e) $R_1 = 100$ kΩ, $R_2 = 1$ MΩ

D2.12 Using an ideal op amp, what are the values of the resistors R_1 and R_2 to be used to design amplifiers with the closed-loop gains listed below? In your designs, use at least one 10-kΩ resistor and another larger resistor.

(a) −1 V/V
(b) −2 V/V
(c) −0.5 V/V
(d) −100 V/V

D2.13 Design an inverting op-amp circuit for which the gain is −5 V/V and the total resistance used is 120 kΩ.

D2.14 Using the circuit of Fig. 2.5 and assuming an ideal op amp, design an inverting amplifier with a gain of 26 dB having the largest possible input resistance under the constraint of having to use resistors no larger than 10 MΩ. What is the input resistance of your design?

2.15 An ideal op amp connected as shown in Fig. 2.5 of the text with $R_1 = 10$ kΩ and $R_2 = 100$ kΩ. A symmetrical square-wave signal with levels of 0 V and 1 V is applied at the input. Sketch and clearly label the waveform of the resulting output voltage. What is its average value? What is its highest value? What is its lowest value?

2.16 For the circuit in Fig. P2.16, find the currents through all branches and the voltages at all nodes. Since the current supplied by the op amp is greater than the current drawn from the input signal source, where does the additional current come from?

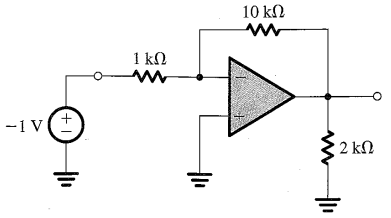

FIGURE P2.16

2.17 An inverting op amp circuit is fabricated with the resistors R_1 and R_2 having x% tolerance (i.e., the value of each resistance can deviate from the nominal value by as much as $\pm x$%). What is the tolerance on the realized closed-loop gain? Assume the op amp to be ideal. If the nominal closed-loop gain is −100 V/V and $x = 5$, what is the range of gain values expected from such a circuit?

2.18 An ideal op amp with 5-kΩ and 15-kΩ resistors is used to create a +5-V supply from a −15-V reference. Sketch the circuit. What are the voltages at the ends of the 5-kΩ resistor? If these resistors are so-called 1% resistors, whose actual values are the range bounded by the nominal value ±1%, what are the limits of the output voltage produced? If the −15-V supply can also vary by ±1%, what is the range of the output voltages that might be found?

2.19 An inverting op-amp circuit for which the required gain is −50 V/V uses an op amp whose open-loop gain is only 200 V/V. If the larger resistor used is 100 kΩ, to what must the smaller be adjusted? With what resistor must a 2-kΩ resistor connected to the input be shunted to achieved this goal? (Note that a resistor R_a is said to be shunted by resistor R_b when R_b is placed in parallel with R_a.)

D2.20 (a) Design an inverting amplifier with a closed-loop gain of −100 V/V and an input resistance of 1 kΩ.
(b) If the op amp is known to have an open-loop gain of 1000 V/V, what do you expect the closed-loop gain of your circuit to be (assuming the resistors have precise values)?
(c) Give the value of a resistor you can place in parallel (shunt) with R_1 to restore the closed-loop gain to its nominal value. Use the closest standard 1% resistor value (see Appendix G).

2.21 An op amp with an open-loop gain of 1000 V/V is used in the inverting configuration. If in this application the output voltage ranges from −10 V to +10 V, what is the maximum voltage by which the "virtual ground node" departs from its ideal value?

2.22 The circuit in Fig. P2.22 is frequently used to provide an output voltage v_o proportional to an input signal current i_i. Derive expressions for the transresistance $R_m \equiv v_o/i_i$ and the input resistance $R_i \equiv v_i/i_i$ for the following cases:

(a) A is infinite.
(b) A is finite.

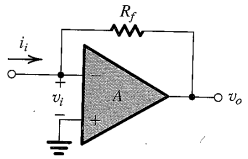

FIGURE P2.22

2.23 Derive an expression for the input resistance of the inverting amplifier of Fig. 2.5 taking into account the finite open-loop gain A of the op amp.

***2.24** For an inverting op amp with open-loop gain A and nominal closed-loop gain R_2/R_1, find the minimum value the gain A must have (in terms of R_2/R_1) for a gain error of 0.1%, 1%, and 10%. In each case, what value of resistor R_{1a} can be used to shunt R_1 to achieve the nominal result?

***2.25** Figure P2.25 shows an op amp that is ideal except for having a finite open-loop gain and is used to realize an inverting amplifier whose gain has a nominal magnitude $G = R_2/R_1$. To compensate for the gain reduction due to the finite A, a resistor R_c is shunted across R_1. Show that perfect compensation is achieved when R_c is selected according to

$$\frac{R_c}{R_1} = \frac{A-G}{1+G}$$

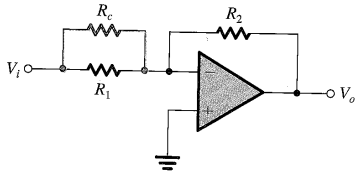

FIGURE P2.25

***2.26** Rearrange Eq. (2.5) to give the amplifier open-loop gain A required to realize a specified closed-loop gain ($G_{\text{nominal}} = -R_2/R_1$) within a specified gain error ε,

$$\varepsilon \equiv \left|\frac{G - G_{\text{nominal}}}{G_{\text{nominal}}}\right|$$

For a closed-loop gain of −100 and a gain error of ≤10%, what is the minimum A required?

***2.27** Using Eq. (2.5), determine the value of A for which a reduction of A by x% results in a reduction in $|G|$ by (x/k)%. Find the value of A required for the case in which the nominal closed-loop gain is 100, x is 50, and k is 100.

2.28 Consider the circuit in Fig. 2.8 with $R_1 = R_2 = R_4 = 1$ MΩ, and assume the op amp to be ideal. Find values for R_3 to obtain the following gains:

(a) −10 V/V
(b) −100 V/V
(c) −2 V/V

D2.29 An inverting op-amp circuit using an ideal op amp must be designed to have a gain of −1000 V/V using resistors no larger than 100 kΩ.

(a) For the simple two-resistor circuit, what input resistance would result?
(b) If the circuit in Fig. 2.8 is used with three resistors of maximum value, what input resistance results? What is the value of the smallest resistor needed?

2.30 The inverting circuit with the T network in the feedback is redrawn in Fig. P2.30 in a way that emphasizes the observation that R_2 and R_3 in effect are in parallel (because the ideal op amp forces a virtual ground at the inverting input terminal). Use this observation to derive an expression for the gain (v_O/v_I) by first finding (v_X/v_I) and (v_O/v_X).

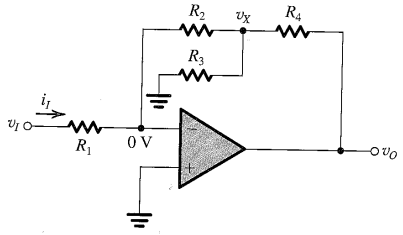

FIGURE P2.30

***2.31** The circuit in Fig. P2.31 can be considered an extension of the circuit in Fig. 2.8.

(a) Find the resistances looking into node 1, R_1; node 2, R_2; node 3, R_3; and node 4, R_4.
(b) Find the currents I_1, I_2, I_3, and I_4 in terms of the input current I.

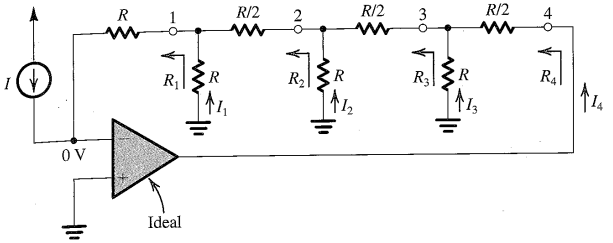

FIGURE P2.31

(c) Find the voltages at nodes 1, 2, 3, and 4, that is, V_1, V_2, V_3, and V_4 in terms of (IR).

2.32 The circuit in Fig. P2.32 utilizes an ideal op amp.

(a) Find I_1, I_2, I_3, and V_x.
(b) If V_O is not to be lower than −13 V, find the maximum allowed value for R_L.
(c) If R_L is varied in the range 100 Ω to 1 kΩ, what is the corresponding change in I_L and in V_O?

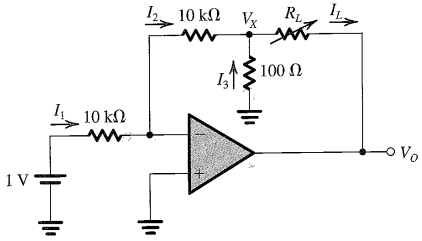

FIGURE P2.32

D2.33 Assuming the op amp to be ideal, it is required to design the circuit shown in Fig. P2.33 to implement a current amplifier with gain $i_L/i_I = 20$ A/A.

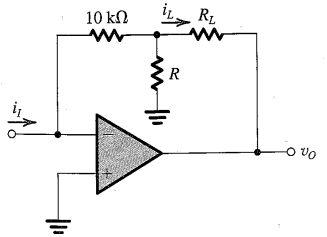

FIGURE P2.33

(a) Find the required value for R.
(b) If $R_L = 1$ kΩ and the op amp operates in an ideal manner so long as v_O is in the range ±12 V. What range of i_I is possible?
(c) What is the input resistance of the current amplifier? If the amplifier is fed with a current source having a current of 1 mA and a source resistance of 10 kΩ, find i_L.

2.34 Figure P2.34 shows the inverting amplifier circuit of Fig. 2.8 redrawn to emphasize the fact that R_3 and R_4 can be thought of as a voltage divider connected across the output v_O and from which a fraction of the output voltage (that available at node A) is fed back through R_2. Assuming $R_2 \gg R_3$ and thus that the loading of the feedback network can be ignored, express v_A as a function of v_O. Now express v_A as a function of v_I. Use these two relationships to find the (approximate) relationship between v_O and v_I. With appropriate manipulation, compare it with the result obtained in Example 2.2. Show that the exact result can be obtained by noting that R_2 appears in effect across R_3 and, thus, that the voltage divider is composed of R_4 and $(R_3 \parallel R_2)$.

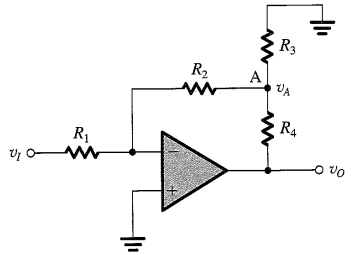

FIGURE P2.34

D2.35 Design the circuit shown in Fig. P2.35 to have an input resistance of 100 kΩ and a gain that can be varied from −1 V/V to −10 V/V using the 10-kΩ potentiometer R_4. What

voltage gain results when the potentiometer is set exactly at its middle value?

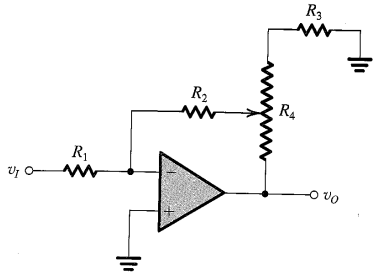

FIGURE P2.35

2.36 A weighted summer circuit using an ideal op amp has three inputs using 100-kΩ resistors and a feedback resistor of 50 kΩ. A signal v_1 is connected to two of the inputs while a signal v_2 is connected to the third. Express v_O in terms of v_1 and v_2. If $v_1 = 3$ V and $v_2 = -3$ V, what is v_O?

D2.37 Design an op amp circuit to provide an output $v_O = -[4v_1 + (v_2/3)]$. Choose relatively low values of resistors but ones for which the input current (from each input signal source) does not exceed 0.1 mA for 1-V input signals.

D2.38 Using the scheme illustrated in Fig. 2.10, design an op-amp circuit with inputs v_1, v_2, and v_3 whose output is $v_O = -(2v_1 + 4v_2 + 8v_3)$ using small resistors but no smaller than 10 kΩ.

D2.39 An ideal op amp is connected in the weighted summer configuration of Fig. 2.10. The feedback resistor R_f = 10 kΩ, and six 10-kΩ resistors are connected to the inverting input terminal of the op amp. Show, by sketching the various circuit configurations, how this basic circuit can be used to implement the following functions:

(a) $v_O = -(v_1 + 2v_2 + 3v_3)$
(b) $v_O = -(v_1 + v_2 + 2v_3 + 2v_4)$
(c) $v_O = -(v_1 + 5v_2)$
(d) $v_O = -6v_1$

In each case find the input resistance seen by each of the signal sources supplying v_1, v_2, v_3, and v_4. Suggest at least two additional summing functions that you can realize with this circuit. How would you realize a summing coefficient that is 0.5?

D2.40 Give a circuit, complete with component values, for a weighted summer that shifts the dc level of a sine-wave signal of 5 sin(ωt) V from zero to −5 V. Assume that in addition to the sine-wave signal you have a dc reference voltage of 2 V available. Sketch the output signal waveform.

D2.41 Use two ideal op amps and resistors to implement the summing function.

$$v_O = v_1 + 2v_2 - 3v_3 - 4v_4$$

D*2.42 In an instrumentation system, there is a need to take the difference between two signals, one of $v_1 = 3\sin(2\pi \times 60t) + 0.01\sin(2\pi \times 1000t)$, volts and another of $v_2 = 3\sin(2\pi \times 60t) - 0.01\sin(2\pi \times 1000t)$ volts. Draw a circuit that finds the required difference using two op amps and mainly 10-kΩ resistors. Since it is desirable to amplify the 1000-Hz component in the process, arrange to provide an overall gain of 10 as well. The op amps available are ideal except that their output voltage swing is limited to ±10 V.

***2.43** Figure P2.43 shows a circuit for a digital-to-analog converter (DAC). The circuit accepts a 4-bit input binary word $a_3a_2a_1a_0$, where a_0, a_1, a_2, and a_3 take the values of 0 or 1, and it provides an analog output voltage v_O proportional to the value of the digital input. Each of the bits of the input word controls the correspondingly numbered switch. For instance, if a_2 is 0 then switch S_2 connects the 20-kΩ resistor to ground, while if a_2 is 1 then S_2 connects the 20-kΩ resistor to the +5-V power supply. Show that v_O is given by

$$v_O = -\frac{R_f}{16}[2^0a_0 + 2^1a_1 + 2^2a_2 + 2^3a_3]$$

where R_f is in kΩ. Find the value of R_f so that v_O ranges from 0 to −12 volts.

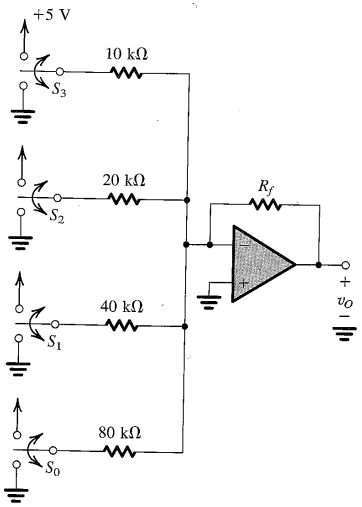

FIGURE P2.43

SECTION 2.3: THE NONINVERTING CONFIGURATION

D2.44 Using an ideal op amp to implement designs for the following closed-loop gains, what values of resistors (R_1, R_2) should be used? Where possible, use at least one 10-kΩ resistor as the smallest resistor in your design.

(a) +1 V/V
(b) +2 V/V
(c) +101 V/V
(d) +100 V/V

D2.45 Design a circuit based on the topology of the noninverting amplifier to obtain a gain of +1.5 V/V, using only 10-kΩ resistors. Note that there are two possibilities. Which of these can be easily converted to have a gain of either +1.0 V/V or +2.0 V/V simply by short-circuiting a single resistor in each case?

D2.46 Figure P2.46 shows a circuit for an analog voltmeter of very high input resistance that uses an inexpensive moving-coil meter. The voltmeter measures the voltage V applied between the op amp's positive-input terminal and ground. Assuming that the moving coil produces full-scale deflection when the current passing through it is 100 μA, find the value of R such that full-scale reading is obtained when V is +10 V. Does the meter resistance shown affect the voltmeter calibration?

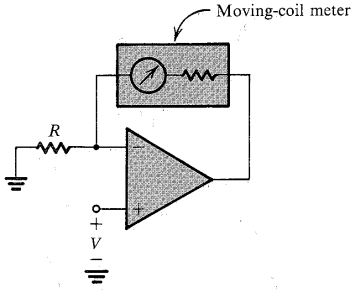

FIGURE P2.46

D*2.47 (a) Use superposition to show that the output of the circuit in Fig. P2.47 is given by

$$v_O = -\left[\frac{R_f}{R_{N1}}v_{N1} + \frac{R_f}{R_{N2}}v_{N2} + \cdots + \frac{R_f}{R_{Nn}}v_{Nn}\right] + \left[1 + \frac{R_f}{R_N}\right]\left[\frac{R_P}{R_{P1}}v_{P1} + \frac{R_P}{R_{P2}}v_{P2} + \cdots + \frac{R_P}{R_{Pn}}v_{Pn}\right]$$

where $R_N = R_{N1}//R_{N2}// \cdots //R_{Nn}$ and
$R_P = R_{P1}//R_{P2}// \cdots //R_{Pn}//R_{P0}$

(b) Design a circuit to obtain

$$v_O = -2v_{N1} + v_{P1} + 2v_{P2}$$

The smallest resistor used should be 10 kΩ.

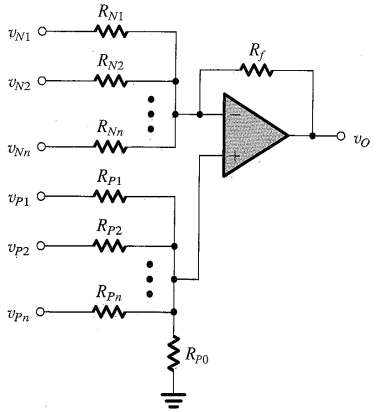

FIGURE P2.47

D2.48 Design a circuit, using one ideal op amp, whose output is $v_O = v_{I1} + 3v_{I2} - 2(v_{I3} + 3v_{I4})$. (*Hint:* Use a structure similar to that shown in general form in Fig. P2.47.)

2.49 Derive an expression for the voltage gain, v_O/v_I, of the circuit in Fig. P2.49.

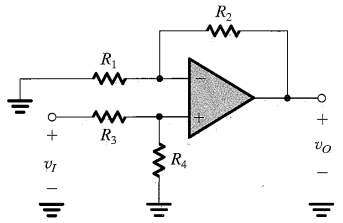

FIGURE P2.49

2.50 For the circuit in Fig. P2.50, use superposition to find v_O in terms of the input voltages v_1 and v_2. Assume an ideal op amp. For

$v_1 = 10\sin(2\pi \times 60t) - 0.1\sin(2\pi \times 1000t)$, volts
$v_2 = 10\sin(2\pi \times 60t) + 0.1\sin(2\pi \times 1000t)$, volts

find v_O.