bias current of 1 $\mu$A and an offset current of 0.1 $\mu$A, what range of outputs would you expect? Indicate where you would add an additional resistor to compensate for the bias currents. What does the range of possible outputs then become? A designer wishes to use this amplifier with a 15-k$\Omega$ source. In order to compensate for the bias current in this case, what resistor would you use? And where?

**D2.106** The circuit of Fig. 2.36 is used to create an ac-coupled noninverting amplifier with a gain of 200 V/V using resistors no larger than 100 k$\Omega$. What values of $R_1$, $R_2$, and $R_3$ should be used? For a break frequency due to $C_1$ at 100 Hz, and that due to $C_2$ at 10 Hz, what values of $C_1$ and $C_2$ are needed?

***2.107** Consider the difference amplifier circuit in Fig. 2.16. Let $R_1 = R_3 = 10$ k$\Omega$ and $R_2 = R_4 = 1$ M$\Omega$. If the op amp has $V_{OS} = 4$ mV, $I_B = 0.3$ $\mu$A, and $I_{OS} = 50$ nA, find the worst-case (largest) dc offset voltage at the output.

***2.108** The circuit shown in Fig. P2.108 uses an op amp having a ±4-mV offset. What is its output offset voltage? What does the output offset become with the input ac coupled through a capacitor $C$? If, instead, the 1-k$\Omega$ resistor is capacitively coupled to ground, what does the output offset become?

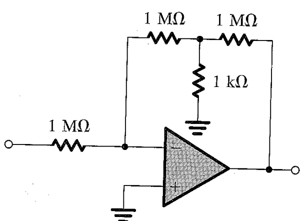


**FIGURE P2.108**

**2.109** Using offset-nulling facilities provided for the op amp, a closed-loop amplifier with gain of +1000 is adjusted at 25°C to produce zero output with the input grounded. If the input offset-voltage drift of the op amp is specified to be 10 $\mu$V/°C, what output would you expect at 0°C and at 75°C? While nothing can be said separately about the polarity of the output offset at either 0 or 75°C, what would you expect their relative polarities to be?

**2.110** An op amp is connected in a closed loop with gain of +100 utilizing a feedback resistor of 1 M$\Omega$.

(a) If the input bias current is 100 nA, what output voltage results with the input grounded?

(b) If the input offset voltage is ±1 mV and the input bias current as in (a), what is the largest possible output that can be observed with the input grounded?

(c) If bias-current compensation is used, what is the value of the required resistor? If the offset current is no more than one-tenth the bias current, what is the resulting output offset voltage (due to offset current alone)?

(d) With bias-current compensation as in (c) in place what is the largest dc voltage at the output due to the combined effect of offset voltage and offset current?

***2.111** An op amp intended for operation with a closed-loop gain of –100 V/V uses feedback resistors of 10 k$\Omega$ and 1 M$\Omega$ with a bias-current-compensation resistor $R_3$. What should the value of $R_3$ be? With input grounded, the output offset voltage is found to be +0.21 V. Estimate the input offset current assuming zero input offset voltage. If the input offset voltage can be as large as 1 mV of unknown polarity, what range of offset current is possible? What current injected into, or extracted from, the nongrounded end of $R_3$ would reduce the op amp output voltage to zero? For available ±15-V supplies, what resistor and supply voltage would you use?

## SECTION 2.8: INTEGRATORS AND DIFFERENTIATORS

**2.112** A Miller integrator incorporates an ideal op amp, a resistor $R$ of 100 k$\Omega$, and a capacitor $C$ of 10 nF. A sine-wave signal is applied to its input.

(a) At what frequency (in Hz) are the input and output signals equal in amplitude?

(b) At that frequency how does the phase of the output sine wave relate to that of the input?

(c) If the frequency is lowered by a factor of 10 from that found in (a), by what factor does the output voltage change, and in what direction (smaller or larger)?

(d) What is the phase relation between the input and output in situation (c)?

**D2.113** Design a Miller integrator with a time constant of one second and an input resistance of 100 k$\Omega$. For a dc voltage of –1 volt applied at the input at time 0, at which moment $v_O = -10$ V, how long does it take the output to reach 0 V? +10 V?

**2.114** An op-amp-based inverting integrator is measured at 1 kHz to have a voltage gain of –100 V/V. At what frequency is its gain reduced to –1 V/V? What is the integrator time constant?

**D2.115** Design a Miller integrator that has a unity-gain frequency of 1 krad/s and an input resistance of 100 k$\Omega$. Sketch the output you would expect for the situation in which, with output initially at 0 V, a 2-V 2-ms pulse is applied to the input. Characterize the output that results when a sine wave 2 sin 1000$t$ is applied to the input?

**D2.116** Design a Miller integrator whose input resistance is 20 k$\Omega$ and unity-gain frequency is 10 kHz. What components are needed? For long-term stability, a feedback resistor is introduced across the capacitor, which limits the dc gain to 40 dB. What is its value? What is the associated lower 3-dB frequency? Sketch and label the output which results with a 0.1-ms, 1-V positive-input pulse (initially at 0 V) with (a) no dc stabilization (but with the output initially at 0 V) and (b) the feedback resistor connected.

***2.117** A Miller integrator whose input and output voltages are initially zero and whose time constant is 1 ms is driven by the signal shown in Fig. P2.117. Sketch and label the output waveform that results. Indicate what happens if the input levels are ±2 V, with the time constant the same (1 ms) and with the time constant raised to 2 ms.

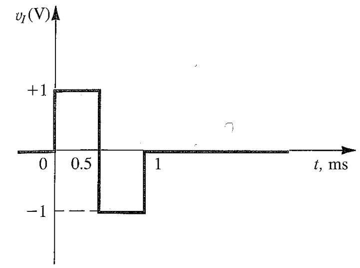


**FIGURE P2.117**

**2.118** Consider a Miller integrator having a time constant of 1 ms, and whose output is initially zero, when fed with a string of pulses of 10-$\mu$s duration and 1-V amplitude rising from 0 V (see Fig. P2.118). Sketch and label the output waveform resulting. How many pulses are required for an output voltage change of 1 V?

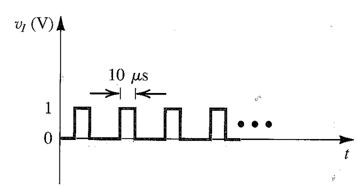


**FIGURE P2.118**

**D2.119** Figure P2.119 shows a circuit that performs a low-pass STC function. Such a circuit is known as a first-order low-pass active filter. Derive the transfer function and show that the dc gain is $(-R_2/R_1)$ and the 3-dB frequency $\omega_0 = 1/CR_2$. Design the circuit to obtain an input resistance of 1 k$\Omega$, a dc gain of 20 dB, and a 3-dB frequency of 4 kHz. At what frequency does the magnitude of the transfer function reduce to unity?

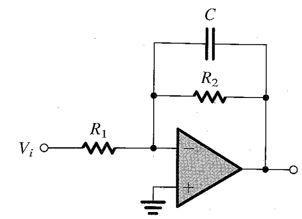


**FIGURE P2.119**

**2.120** A Miller integrator with $R = 10$ k$\Omega$ and $C = 10$ nF is implemented using an op amp with $V_{OS} = 3$ mV, $I_B = 0.1$ $\mu$A, and $I_{OS} = 10$ nA. To provide a finite dc gain, a 1-M$\Omega$ resistor is connected across the capacitor.

(a) To compensate for the effect of $I_B$, a resistor is connected in series with the positive-input terminal of the op amp. What should its value be?

(b) With the resistor of (a) in place, find the worst-case dc output voltage of the integrator when the input is grounded.

**2.121** A differentiator utilizes an ideal op amp, a 10-k$\Omega$ resistor, and a 0.01-$\mu$F capacitor. What is the frequency $f_0$ (in Hz) at which its input and output sine-wave signals have equal magnitude? What is the output signal for a 1-V peak-to-peak sine-wave input with frequency equal to $10f_0$?

**2.122** An op-amp differentiator with 1-ms time constant is driven by the rate-controlled step shown in Fig. P2.122. Assuming $v_O$ to be zero initially, sketch and label its waveform.

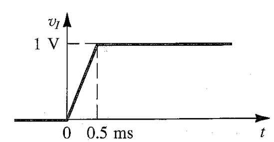


**FIGURE P2.122**

***2.123** An op-amp differentiator, employing the circuit shown in Fig. 2.44(a), has $R = 10$ k$\Omega$ and $C = 0.1$ $\mu$F. When a triangle wave of ±1-V peak amplitude at 1 kHz is applied to the input, what form of output results? What is its frequency? What is its peak amplitude? What is its average value? What value of $R$ is needed to cause the output to have a 10-V peak amplitude? When a 1-V peak sine wave at 1 kHz is applied to