

**\*D3.70** A zener shunt regulator employs a 9.1-V zener diode for which  $V_Z = 9.1$  V at  $I_Z = 9$  mA, with  $r_z = 30$   $\Omega$  and  $I_{ZK} = 0.3$  mA. The available supply voltage of 15 V can vary as much as  $\pm 10\%$ . For this diode, what is the value of  $V_{O20}$ ? For a nominal load resistance  $R_L$  of 1 k $\Omega$  and a nominal zener current of 10 mA, what current must flow in the supply resistor  $R$ ? For the nominal value of supply voltage, select a value for resistor  $R$ , specified to one significant digit, to provide at least that current. What nominal output voltage results? For a  $\pm 10\%$  change in the supply voltage, what variation in output voltage results? If the load current is reduced by 50%, what increase in  $V_O$  results? What is the smallest value of load resistance that can be tolerated while maintaining regulation when the supply voltage is low? What is the lowest possible output voltage that results? Calculate values for the line regulation and for the load regulation for this circuit using the numerical results obtained in this problem.

**\*D3.71** It is required to design a zener shunt regulator to provide a regulated voltage of about 10 V. The available 10-V, 1-W zener of type 1N4740 is specified to have a 10-V drop at a test current of 25 mA. At this current its  $r_z$  is 7  $\Omega$ . The raw supply available has a nominal value of 20 V but can vary by as much as  $\pm 25\%$ . The regulator is required to supply a load current of 0 mA to 20 mA. Design for a minimum zener current of 5 mA.

- Find  $V_{O20}$ .
- Calculate the required value of  $R$ .
- Find the line regulation. What is the change in  $V_O$  expressed as a percentage, corresponding to the  $\pm 25\%$  change in  $V_S$ ?
- Find the load regulation. By what percentage does  $V_O$  change from the no-load to the full-load condition?
- What is the maximum current that the zener in your design is required to conduct? What is the zener power dissipation under this condition?

### SECTION 3.5: RECTIFIER CIRCUITS

**3.72** Consider the half-wave rectifier circuit of Fig. 3.25(a) with the diode reversed. Let  $v_S$  be a sinusoid with 15-V peak amplitude, and let  $R = 1.5$  k $\Omega$ . Use the constant-voltage-drop diode model with  $V_D = 0.7$  V.

- Sketch the transfer characteristic.
- Sketch the waveform of  $v_O$ .
- Find the average value of  $v_O$ .
- Find the peak current in the diode.
- Find the PIV of the diode.

**3.73** Using the exponential diode characteristic, show that for  $v_S$  and  $v_O$  both greater than zero, the circuit of Fig. 3.25(a) has the transfer characteristic

$$v_O = v_S - v_D \quad (\text{at } i_D = 1 \text{ mA}) - nV_T \ln(v_O/R)$$

where  $v_S$  and  $v_O$  are in volts and  $R$  is in kilohms.

**3.74** Consider a half-wave rectifier circuit with a triangular-wave input of 5-V peak-to-peak amplitude and zero average and with  $R = 1$  k $\Omega$ . Assume that the diode can be represented by the piecewise-linear model with  $V_{D0} = 0.65$  V and  $r_D = 20$   $\Omega$ . Find the average value of  $v_O$ .

**3.75** For a half-wave rectifier circuit with  $R = 1$  k $\Omega$ , utilizing a diode whose voltage drop is 0.7 V at a current of 1 mA and exhibiting a 0.1-V change per decade of current variation, find the values of the input voltage to the rectifier corresponding to  $v_O = 0.1$  V, 0.5 V, 1 V, 2 V, 5 V, and 10 V. Plot the rectifier transfer characteristic.

**3.76** A half-wave rectifier circuit with a 1-k $\Omega$  load operates from a 120-V (rms) 60-Hz household supply through a 10-to-1 step-down transformer. It uses a silicon diode that can be modeled to have a 0.7-V drop for any current. What is the peak voltage of the rectified output? For what fraction of the cycle does the diode conduct? What is the average output voltage? What is the average current in the load?

**3.77** A full-wave rectifier circuit with a 1-k $\Omega$  load operates from a 120-V (rms) 60-Hz household supply through a 5-to-1 transformer having a center-tapped secondary winding. It uses two silicon diodes that can be modeled to have a 0.7-V drop for all currents. What is the peak voltage of the rectified output? For what fraction of a cycle does each diode conduct? What is the average output voltage? What is the average current in the load?

**3.78** A full-wave bridge rectifier circuit with a 1-k $\Omega$  load operates from a 120-V (rms) 60-Hz household supply through a 10-to-1 step-down transformer having a single secondary winding. It uses four diodes, each of which can be modeled to have a 0.7-V drop for any current. What is the peak value of the rectified voltage across the load? For what fraction of a cycle does each diode conduct? What is the average voltage across the load? What is the average current through the load?

**D3.79** It is required to design a full-wave rectifier circuit using the circuit of Fig. 3.26 to provide an average output voltage of:

- 10 V
- 100 V

In each case find the required turns ratio of the transformer. Assume that a conducting diode has a voltage drop of 0.7 V. The ac line voltage is 120 V rms.

**D3.80** Repeat Problem 3.79 for the bridge rectifier circuit of Fig. 3.27.

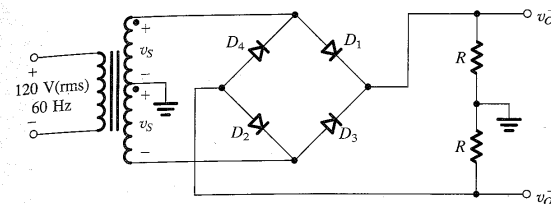


FIGURE P3.82

**D3.81** Consider the full-wave rectifier in Fig. 3.26 when the transformer turns ratio is such that the voltage across the entire secondary winding is 24 V rms. If the input ac line voltage (120 V rms) fluctuates by as much as  $\pm 10\%$ , find the required PIV of the diodes. (Remember to use a factor of safety in your design.)

**\*3.82** The circuit in Fig. P3.82 implements a complementary-output rectifier. Sketch and clearly label the waveforms of  $v_O^+$  and  $v_O^-$ . Assume a 0.7-V drop across each conducting diode. If the magnitude of the average of each output is to be 15 V, find the required amplitude of the sine wave across the entire secondary winding. What is the PIV of each diode?

**3.83** Augment the rectifier circuit of Problem 3.76 with a capacitor chosen to provide a peak-to-peak ripple voltage of (i) 10% of the peak output and (ii) 1% of the peak output. In each case:

- What average output voltage results?
- What fraction of the cycle does the diode conduct?
- What is the average diode current?
- What is the peak diode current?

**3.84** Repeat Problem 3.83 for the rectifier in Problem 3.77.

**3.85** Repeat Problem 3.83 for the rectifier in Problem 3.78.

**\*D3.86** It is required to use a peak rectifier to design a dc power supply that provides an average dc output voltage of 15 V on which a maximum of  $\pm 1$ -V ripple is allowed. The rectifier feeds a load of 150  $\Omega$ . The rectifier is fed from the line voltage (120 V rms, 60 Hz) through a transformer. The diodes available have 0.7-V drop when conducting. If the designer opts for the half-wave circuit:

- Specify the rms voltage that must appear across the transformer secondary.
- Find the required value of the filter capacitor.

(c) Find the maximum reverse voltage that will appear across the diode, and specify the PIV rating of the diode.

(d) Calculate the average current through the diode during conduction.

(e) Calculate the peak diode current.

**\*D3.87** Repeat Problem 3.86 for the case in which the designer opts for a full-wave circuit utilizing a center-tapped transformer.

**\*D3.88** Repeat Problem 3.86 for the case in which the designer opts for a full-wave bridge rectifier circuit.

**\*3.89** Consider a half-wave peak rectifier fed with a voltage  $v_S$  having a triangular waveform with 20-V peak-to-peak amplitude, zero average, and 1-kHz frequency. Assume that the diode has a 0.7-V drop when conducting. Let the load resistance  $R = 100$   $\Omega$  and the filter capacitor  $C = 100$   $\mu$ F. Find the average dc output voltage, the time interval during which the diode conducts, the average diode current during conduction, and the maximum diode current.

**\*D3.90** Consider the circuit in Fig. P3.82 with two equal filter capacitors placed across the load resistors  $R$ . Assume that the diodes available exhibit a 0.7-V drop when conducting. Design the circuit to provide  $\pm 15$ -V dc output voltages with a peak-to-peak ripple no greater than 1 V. Each supply should be capable of providing 200 mA dc current to its load resistor  $R$ . Completely specify the capacitors, diodes and the transformer.

**3.91** The op amp in the precision rectifier circuit of Fig. P3.91 is ideal with output saturation levels of  $\pm 12$  V. Assume that when conducting the diode exhibits a constant voltage drop of 0.7 V. Find  $v_+$ ,  $v_O$ , and  $v_A$  for:

- $v_I = +1$  V
- $v_I = +2$  V
- $v_I = -1$  V
- $v_I = -2$  V

Also, find the average output voltage obtained when  $v_I$  is a symmetrical square wave of 1-kHz frequency, 5-V amplitude, and zero average.

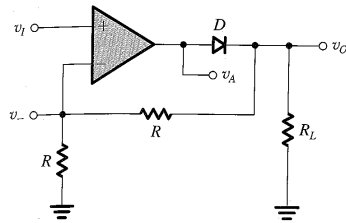


FIGURE P3.91

**3.92** The op amp in the circuit of Fig. P3.92 is ideal with output saturation levels of  $\pm 12$  V. The diodes exhibit a constant 0.7-V drop when conducting. Find  $v_+$ ,  $v_A$ , and  $v_O$  for:

- (a)  $v_I = +1$  V
- (b)  $v_I = +2$  V
- (c)  $v_I = -1$  V
- (d)  $v_I = -2$  V

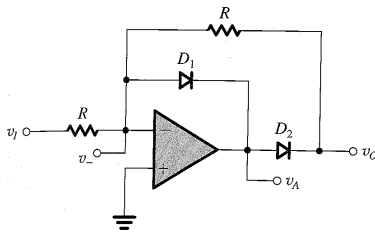


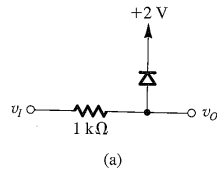
FIGURE P3.92

**SECTION 3.6: LIMITING AND CLAMPING CIRCUITS**

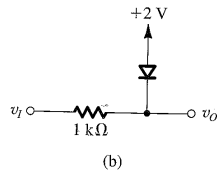
**3.93** Sketch the transfer characteristic  $v_O$  versus  $v_I$  for the limiter circuits shown in Fig. P3.93. All diodes begin conducting at a forward voltage drop of 0.5 V and have voltage drops of 0.7 V when fully conducting.

**3.94** Repeat Problem 3.93 assuming that the diodes are modeled with the piecewise-linear model with  $V_{D0} = 0.65$  V and  $r_D = 20$   $\Omega$ .

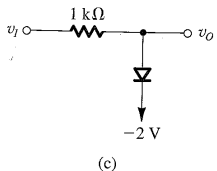
**3.95** The circuits in Fig. P3.93(a) and (d) are connected as follows: The two input terminals are tied together, and the



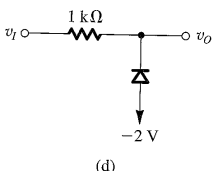
(a)



(b)



(c)



(d)

FIGURE P3.93

two output terminals are tied together. Sketch the transfer characteristic of the circuit resulting, assuming that the cut-in voltage of the diodes is 0.5 V and their voltage drop when fully conducting is 0.7 V.

**3.96** Repeat Problem 3.95 for the two circuits in Fig. P3.93(a) and (b) connected together as follows: The two input terminals are tied together, and the two output terminals are tied together.

**\*3.97** Sketch and clearly label the transfer characteristic of the circuit in Fig. P3.97 for  $-20$  V  $\leq v_I \leq +20$  V. Assume that the diodes can be represented by a piecewise-linear model with  $V_{D0} = 0.65$  V and  $r_D = 20$   $\Omega$ . Assuming that the specified

zener voltage (8.2 V) is measured at a current of 10 mA and that  $r_z = 20$   $\Omega$ , represent the zener by a piecewise-linear model.

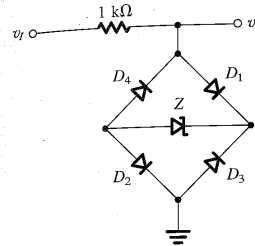


FIGURE P3.97

**\*3.98** Plot the transfer characteristic of the circuit in Fig. P3.98 by evaluating  $v_I$  corresponding to  $v_O = 0.5$  V, 0.6 V, 0.7 V, 0.8 V, 0 V,  $-0.5$  V,  $-0.6$  V,  $-0.7$  V, and  $-0.8$  V. Assume that the diodes are 1-mA units (i.e., have 0.7-V drops at 1-mA currents) having a 0.1-V/decade logarithmic characteristic. Characterize the circuit as a hard or soft limiter. What is the value of  $K$ ? Estimate  $L_+$  and  $L_-$ .

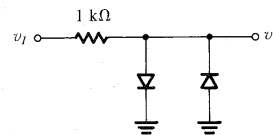


FIGURE P3.98

**D3.99** Design limiter circuits using only diodes and 10-k $\Omega$  resistors to provide an output signal limited to the range:

- (a)  $-0.7$  V and above
- (b)  $-2.1$  V and above
- (c)  $\pm 1.4$  V

Assume that each diode has a 0.7-V drop when conducting.

**D3.100** Design a two-sided limiting circuit using a resistor, two diodes, and two power supplies to feed a 1-k $\Omega$  load with nominal limiting levels of  $\pm 3$  V. Use diodes modeled by a constant 0.7 V. In the nonlimiting region, the circuit voltage gain should be at least 0.95 V/V.

**\*3.101** Reconsider Problem 3.100 with diodes modeled by a 0.5-V offset and a resistor consistent with 10-mA conduction at 0.7 V. Sketch and quantify the output voltage for inputs of  $\pm 10$  V.

**\*3.102** In the circuit shown in Fig. P3.102, the diodes exhibit a 0.7-V drop at 0.1 mA with a 0.1 V/decade characteristic.

For inputs over the range of  $\pm 5$  V, provide a calibrated sketch of the voltages at outputs B and C. For a 5-V peak, 100-Hz sinusoid applied at A, sketch the signals at nodes B and C.

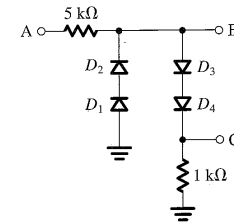


FIGURE P3.102

**\*\*3.103** Sketch and label the transfer characteristic of the circuit shown in Fig. P3.103 over a  $\pm 10$ -V range of input signals. All diodes are 1-mA units (i.e., each exhibits a 0.7-V drop at a current of 1 mA) with  $n = 1$ . What are the slopes of the characteristic at the extreme  $\pm 10$ -V levels?

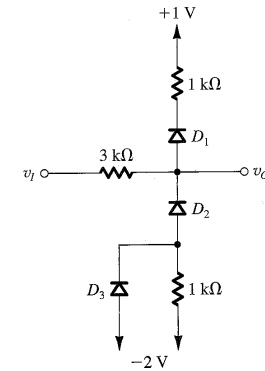


FIGURE P3.103

**3.104** A clamped capacitor using an ideal diode with cathode grounded is supplied with a sine wave of 10-V rms. What is the average (dc) value of the resulting output?

**\*\*3.105** For the circuits in Fig. P3.105, each utilizing an ideal diode (or diodes), sketch the output for the input shown. Label the most positive and most negative output levels. Assume  $CR \gg T$ .