4.48 In the circuit of Fig. P4.48, transistors Q_1 and Q_2 have $V_t = 1$ V, and the process transconductance parameter $k_n' = 100\ \mu A/V^2$. Assuming $\lambda = 0$, find V_1, V_2, and V_3 for each of the following cases:

(a) $(W/L)_1 = (W/L)_2 = 20$
(b) $(W/L)_1 = 1.5(W/L)_2 = 20$

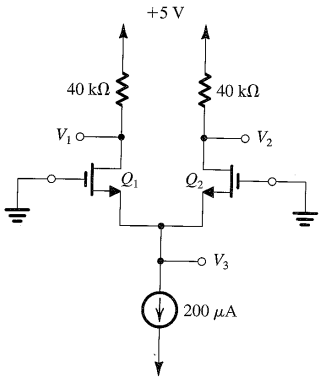

FIGURE P4.48

SECTION 4.4: THE MOSFET AS AN AMPLIFIER AND AS A SWITCH

4.49 Consider the CS amplifier of Fig. 4.26(a) for the case $V_{DD} = 5$ V, $R_D = 24$ kΩ, $k_n'(W/L) = 1$ mA/V^2, and $V_t = 1$ V.

(a) Find the coordinates of the two end points of the saturation-region segment of the amplifier transfer characteristic, that is, points A and B on the sketch of Fig. 4.26(c).
(b) If the amplifier is biased to operate with an overdrive voltage V_{OV} of 0.5 V, find the coordinates of the bias point Q_1 on the transfer characteristic. Also, find the value of I_D and of the incremental gain A_v at the bias point.
(c) For the situation in (b), and disregarding the distortion caused by the MOSFET's square-law characteristic, what is the largest amplitude of a sine-wave voltage signal that can be applied at the input while the transistor remains in saturation? What is the amplitude of the output voltage signal that results? What gain value does the combination of these amplitudes imply? By what percentage is this gain value different from the incremental gain value calculated above? Why is there a difference?

***4.50** We wish to investigate the operation of the CS amplifier circuit studied in Example 4.8 for various bias conditions, that is, for bias at various points along the saturation-region segment of the transfer characteristic. Prepare a table giving the values of I_D (mA), V_{OV} (V), $V_{GS} = V_{IQ}$ (V), A_v (V/V), the magnitude of the largest allowable positive-output signal v_o^+ (V), and the magnitude of the largest allowable negative-output signal v_o^- (V) for values of $V_{DS} = V_{OQ}$ in the range of 1 V to 10 V, in increments of 1 V (i.e., there should be table rows for $V_{DS} = 1$ V, 2 V, 3 V, . . . , 10 V). Note that v_o^+ is determined by the MOSFET entering cutoff and v_o^- by the MOSFET entering the triode region.

4.51 Various measurements are made on an NMOS amplifier for which the drain resistor R_D is 20 kΩ. First, dc measurements show the voltage across the drain resistor, V_{RD}, to be 2 V and the gate-to-source bias voltage to be 1.2 V. Then, ac measurements with small signals show the voltage gain to be −10 V/V. What is the value of V_t for this transistor? If the process transconductance parameter k_n' is 50 μA/V^2, what is the MOSFET's W/L?

***D4.52** Refer to the expression for the incremental voltage gain in Eq. (4.41). Various design considerations place a lower limit on the value of the overdrive voltage V_{OV}. For our purposes here, let this lower limit be 0.2 V. Also, assume that $V_{DD} = 5$ V.

(a) Without allowing any room for output voltage swing, what is the maximum voltage gain achievable?
(b) If we are required to allow for an output voltage swing of ±0.5 V, what dc bias voltage should be established at the drain to obtain maximum gain? What gain value is achievable? What input signal results in a ±0.5-V output swing?
(c) For the situation in (b), find W/L of the transistor to establish a dc drain current of 100 μA. For the given process technology, $k_n' = 100\ \mu A/V^2$.
(d) Find the required value of R_D.

4.53 The expression for the incremental voltage gain A_v given in Eq. (4.41) can be written in as

$$A_v = -\frac{2(V_{DD} - V_{DS})}{V_{OV}}$$

where V_{DS} is the bias voltage at the drain (called V_{OQ} in the text). This expression indicates that for given values of V_{DD} and V_{OV}, the gain magnitude can be increased by biasing the transistor at a lower V_{DS}. This, however, reduces the allowable output signal swing in the negative direction. Assuming linear operation around the bias point, show that the largest possible negative output signal peak $\hat{v}_o$ that is achievable while the transistor remains saturated is

$$\hat{v}_o = (V_{DS} - V_{OV}) \Big/ \left(1 + \frac{1}{A_v}\right)$$

For $V_{DD} = 5$ V and $V_{OV} = 0.5$ V, provide a table of values for A_v, $\hat{v}_o$, and the corresponding $\hat{v}_i$ for $V_{DS} = 1$ V, 1.5 V, 2 V, and 2.5 V. If $k_n'W/L = 1$ mA/V^2, find I_D and R_D for the design for which $V_{DS} = 1$ V.

4.54 Figure P4.54 shows a CS amplifier in which the load resistor R_D has been replaced with another NMOS transistor Q_2 connected as a two-terminal device. Note that because v_{DG} of Q_2 is zero, it will be operating in saturation at all times, even when $v_I = 0$ and $i_{D2} = i_{D1} = 0$. Note also that the two transistors conduct equal drain currents. Using $i_{D1} = i_{D2}$, show that for the range of v_I over which Q_1 is operating in saturation, that is, for

$$V_{t1} \le v_I \le v_O + V_{t1}$$

the output voltage will be given by

$$v_O = V_{DD} - V_t + \sqrt{\frac{(W/L)_1}{(W/L)_2}}\,V_t - \sqrt{\frac{(W/L)_1}{(W/L)_2}}\,v_I$$

where we have assumed $V_{t1} = V_{t2} = V_t$. Thus the circuit functions as a linear amplifier, even for large input signals. For $(W/L)_1 = (50\ \mu m/0.5\ \mu m)$ and $(W/L)_2 = (5\ \mu m/0.5\ \mu m)$, find the voltage gain.

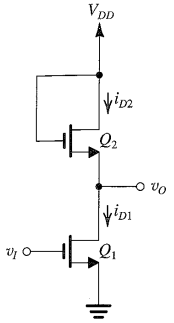

FIGURE P4.54

SECTION 4.5: BIASING IN MOS AMPLIFIER CIRCUITS

D4.55 Consider the classical biasing scheme shown in Fig. 4.30(c), using a 15-V supply. For the MOSFET, $V_t = 1.2$ V, $\lambda = 0$, $k_n' = 80\ \mu A/V^2$, $W = 240\ \mu m$, and $L = 6\ \mu m$. Arrange that the drain current is 2 mA, with about one-third of the supply voltage across each of R_S and R_D. Use 22 MΩ for the larger of R_{G1} and R_{G2}. What are the values of R_{G1}, R_{G2}, R_S, and R_D that you have chosen? Specify them to two significant digits. For your design, how far is the drain voltage from the edge of saturation?

D4.56 Using the circuit topology displayed in Fig. 4.30(e), arrange to bias the NMOS transistor at $I_D = 2$ mA with V_D midway between cutoff and the beginning of triode operation. The available supplies are ±15 V. For the NMOS transistor, $V_t = 0.8$ V, $\lambda = 0$, $k_n' = 50\ \mu A/V^2$, $W = 200\ \mu m$, and $L = 4\ \mu m$. Use a gate-bias resistor of 10 MΩ. Specify R_S and R_D to two significant digits.

***D4.57** In an electronic instrument using the biasing scheme shown in Fig. 4.30(c), a manufacturing error reduces R_S to zero. Let $V_{DD} = 12$ V, $R_{G1} = 5.6$ MΩ, and $R_{G2} = 2.2$ MΩ. What is the value of V_G created? If supplier specifications allow $k_n'(W/L)$ to vary from 220 to 380 μA/V^2 and V_t to vary from 1.3 to 2.4 V, what are the extreme values of I_D that may result? What value of R_S should have been installed to limit the maximum value of I_D to 0.15 mA? Choose an appropriate standard 5% resistor value (refer to Appendix G). What extreme values of current now result?

4.58 An enhancement NMOS transistor is connected in the bias circuit of Fig. 4.30(c), with $V_G = 4$ V and $R_S = 1$ kΩ. The transistor has $V_t = 2$ V and $k_n'(W/L) = 2$ mA/V^2. What bias current results? If a transistor for which $k_n'(W/L)$ is 50% higher is used, what is the resulting percentage increase in I_D?

4.59 The bias circuit of Fig. 4.30(c) is used in a design with $V_G = 5$ V and $R_S = 1$ kΩ. For an enhancement MOSFET with $k_n'(W/L) = 2$ mA/V^2, the source voltage was measured and found to be 2 V. What must V_t be for this device? If a device for which V_t is 0.5 V less is used, what does V_S become? What bias current results?

D4.60 Design the circuit of Fig. 4.30(e) for an enhancement MOSFET having $V_t = 2$ V and $k_n'(W/L) = 2$ mA/V^2. Let $V_{DD} = V_{SS} = 10$ V. Design for a dc bias current of 1 mA and for the largest possible voltage gain (and thus the largest possible R_D) consistent with allowing a 2-V peak-to-peak voltage swing at the drain. Assume that the signal voltage on the source terminal of the FET is zero.

D4.61 Design the circuit in Fig. P4.61 so that the transistor operates in saturation with V_D biased 1 V from the edge of the triode region, with $I_D = 1$ mA and $V_D = 3$ V, for each of the following two devices (use a 10-μA current in the voltage divider):

(a) $|V_t| = 1$ V and $k_p'W/L = 0.5$ mA/V^2
(b) $|V_t| = 2$ V and $k_p'W/L = 1.25$ mA/V^2

For each case, specify the values of V_G, V_D, V_S, R_1, R_2, R_S, and R_D.

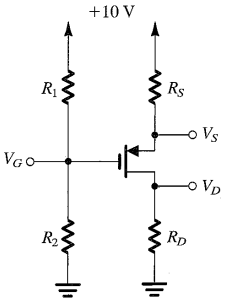

FIGURE P4.61

**D4.62 A very useful way to characterize the stability of the bias current I_D is to evaluate the sensitivity of I_D relative to a particular transistor parameter whose variability might be large. The sensitivity of I_D relative to the MOSFET parameter $K \equiv \frac{1}{2}k'(W/L)$ is defined as

$$S_K^{I_D} \equiv \frac{\delta I_D / I_D}{\delta K / K} = \frac{\delta I_D}{\delta K}\frac{K}{I_D}$$

and its value, when multiplied by the variability (or tolerance) of K, provides the corresponding expected variability of I_D. The purpose of this problem is to investigate the use of the sensitivity function in the design of the bias circuit of Fig. 4.30(e).

(a) Show that for V_t constant,

$$S_K^{I_D} = 1/(1 + 2\sqrt{KI_D}R_S)$$

(b) For a MOSFET having $K = 100\ \mu A/V^2$ with a variability of ±10% and $V_t = 1$ V, find the value of R_S that would result in $I_D = 100\ \mu A$ with a variability of ±1%. Also, find V_{GS} and the required value of V_{SS}.
(c) If the available supply $V_{SS} = 5$ V, find the value of R_S for $I_D = 100\ \mu A$. Evaluate the sensitivity function, and give the expected variability of I_D in this case.

4.63 For the circuit in Fig. 4.33(a) with $I = 1$ mA, $R_G = 0$, $R_D = 5$ kΩ, and $V_{DD} = 10$ V, consider the behavior in each of the following two cases. In each case, find the voltages V_S, V_D, and V_{DS} that result.

(a) $V_t = 1$ V and $k_n'W/L = 0.5$ mA/V^2
(b) $V_t = 2$ V and $k_n'W/L = 1.25$ mA/V^2

4.64 In the circuit of Fig. 4.32, let $R_G = 10$ MΩ, $R_D = 10$ kΩ, and $V_{DD} = 10$ V. For each of the following two transistors, find the voltages V_D and V_G.

(a) $V_t = 1$ V and $k_n'W/L = 0.5$ mA/V^2
(b) $V_t = 2$ V and $k_n'W/L = 1.25$ mA/V^2

D4.65 Using the feedback bias arrangement shown in Fig. 4.32 with a 9-V supply and an NMOS device for which $V_t = 1$ V and $k_n'(W/L) = 0.4$ mA/V^2, find R_D to establish a drain current of 0.2 mA. If resistor values are limited to those on the 5% resistor scale (see Appendix G), what value would you choose? What values of current and V_D result?

D4.66 Figure P4.66 shows a variation of the feedback-bias circuit of Fig. 4.32. Using a 6-V supply with an NMOS transistor for which $V_t = 1.2$ V, $k_n'W/L = 3.2$ mA/V^2 and $\lambda = 0$, provide a design which biases the transistor at $I_D = 2$ mA, with V_{DS} large enough to allow saturation operation for a 2-V negative signal swing at the drain. Use 22 MΩ as the largest resistor in the feedback-bias network. What values of R_D, R_{G1}, and R_{G2} have you chosen? Specify all resistors to two significant digits.

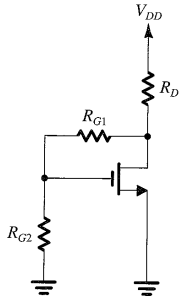

FIGURE P4.66

SECTION 4.6: SMALL-SIGNAL OPERATION AND MODELS

*4.67 This problem investigates the nonlinear distortion introduced by a MOSFET amplifier. Let the signal v_{gs} be a sine wave with amplitude V_{gs}, and substitute $v_{gs} = V_{gs}\sin\omega t$ in Eq. (4.57). Using the trigonometric identity $\sin^2\theta = \frac{1}{2} - \frac{1}{2}\cos 2\theta$, show that the ratio of the signal at frequency 2ω to that at frequency ω, expressed as a percentage (known as the second-harmonic distortion) is

$$\text{Second-harmonic distortion} = \frac{1}{4}\frac{V_{gs}}{V_{OV}} \times 100$$

If in a particular application V_{gs} is 10 mV, find the minimum overdrive voltage at which the transistor should be operated so that the second-harmonic distortion is kept to less than 1%.

4.68 Consider an NMOS transistor having $k_n'W/L = 2$ mA/V^2. Let the transistor be biased at $V_{OV} = 1$ V. For operation in saturation, what dc bias current I_D results? If a +0.1-V signal is superimposed on V_{GS}, find the corresponding increment in collector current by evaluating the total collector current i_D and subtracting the dc bias current I_D. Repeat for a –0.1-V signal. Use these results to estimate g_m of the FET at this bias point. Compare with the value of g_m obtained using Eq. (4.62).

4.69 Consider the FET amplifier of Fig. 4.34 for the case $V_t = 2$ V, $k_n'(W/L) = 1$ mA/V^2, $V_{GS} = 4$ V, $V_{DD} = 10$ V, and $R_D = 3.6$ kΩ.

(a) Find the dc quantities I_D and V_D.
(b) Calculate the value of g_m at the bias point.
(c) Calculate the value of the voltage gain.
(d) If the MOSFET has $\lambda = 0.01$ V^{-1}, find r_o at the bias point and calculate the voltage gain.

*D4.70 An NMOS amplifier is to be designed to provide a 0.50-V peak output signal across a 50-kΩ load that can be used as a drain resistor. If a gain of at least 5 V/V is needed, what g_m is required? Using a dc supply of 3 V, what values of I_D and V_{OV} would you choose? What W/L ratio is required if $\mu_n C_{ox} = 100\ \mu A/V^2$? If $V_t = 0.8$ V, find V_{GS}.

*D4.71 In this problem we investigate an optimum design of the CS amplifier circuit of Fig. 4.34. First, use the voltage gain expression $A_v = -g_m R_D$ together with Eq. (4.71) for g_m to show that

$$A_v = -\frac{2I_D R_D}{V_{OV}} = -\frac{2(V_{DD} - V_D)}{V_{OV}}$$

which is the expression we obtained in Section 4.4 (Eq. 4.41). Next, let the maximum positive input signal be $\hat{v}_i$. To keep the second-harmonic distortion to an acceptable level, we bias the MOSFET to operate at an overdrive voltage $V_{OV} \gg \hat{v}_i$. Let $V_{OV} = m\hat{v}_i$. Now, to maximize the voltage gain $|A_v|$, we design for the lowest possible V_D. Show that the minimum V_D that is consistent with allowing a negative signal voltage swing at the drain of $|A_v|\hat{v}_i$ while maintaining saturation-mode operation is given by

$$V_D = \frac{V_{OV} + \hat{v}_i + 2V_{DD}(\hat{v}_i/V_{OV})}{1 + 2(\hat{v}_i/V_{OV})}$$

Now, find V_{OV}, V_D, A_v, and $\hat{v}_o$ for the case $V_{DD} = 3$ V, $\hat{v}_i = 20$ mV, and $m = 10$. If it is desired to operate this transistor at $I_D = 100\ \mu A$, find the values of R_D and W/L, assuming that for this process technology $k_n' = 100\ \mu A/V^2$.

4.72 In the table below, for enhancement MOS transistors operating under a variety of conditions, complete as many entries as possible. Although some data is not available, it is always possible to calculate g_m using one of Eqs. (4.69), (4.70) or (4.71). In the table, current is in mA, voltage in V, and dimensions in μm. Assume $\mu_n = 500$ cm^2/Vs, $\mu_p = 250$ cm^2/Vs, and $C_{ox} = 0.4$ fF/μm^2.

4.73 An NMOS technology has $\mu_n C_{ox} = 50\ \mu A/V^2$ and $V_t = 0.7$ V. For a transistor with $L = 1$ μm, find the value of W that results in $g_m = 1$ mA/V at $I_D = 0.5$ mA. Also, find the required V_{GS}.

4.74 For the NMOS amplifier in Fig. P4.74, replace the transistor with its T equivalent circuit of Fig. 4.39(d). Derive expressions for the voltage gains v_s/v_i and v_d/v_i.

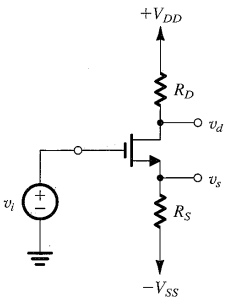

FIGURE P4.74

4.75 In the circuit of Fig. P4.75, the NMOS transistor has $|V_t| = 0.9$ V and $V_A = 50$ V and operates with $V_D = 2$ V. What is the voltage gain v_o/v_i? What do V_D and the gain become for I increased to 1 mA?

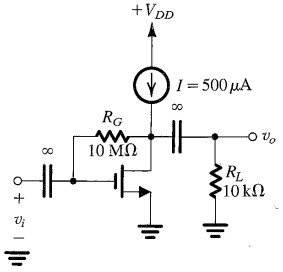

FIGURE P4.75

Case	Type	I_D	$\lvert V_{GS}\rvert$	$\lvert V_t\rvert$	V_{OV}	W	L	W/L	$k'(W/L)$	g_m
a	N	1	3	2			1			
b	N	1		0.7	0.5	50				
c	N	10			2		1			
d	N	0.5			0.5					
e	N	0.1				10	2			
f	N		1.8	0.8		40	4			
g	P	1			2			25		
h	P		3	1					500	
i	P	10				4000	2			
j	P	10			4					
k	P				1	30	3			
l	P	0.1			5				8	