4.76 For a 0.8-μm CMOS fabrication process: $V_{tn} = 0.8$ V, $V_{tp} = -0.9$ V, $\mu_n C_{ox} = 90\ \mu A/V^2$, $\mu_p C_{ox} = 30\ \mu A/V^2$, $C_{ox} = 1.9$ fF/μm^2, $\phi_f = 0.34$ V, $\gamma = 0.5\ V^{1/2}$, V_A (n-channel devices) = $8L$ (μm), and $|V_A|$ (p-channel devices) = $12L$ (μm). Find the small-signal model parameters (g_m, r_o, and g_{mb}) for both an NMOS and a PMOS transistor having $W/L = 20\ \mu m/2\ \mu m$ and operating at $I_D = 100\ \mu A$ with $|V_{SB}| = 1$ V. Also, find the overdrive voltage at which each device must be operating.

4.77 Figure P4.77 shows a discrete-circuit CS amplifier employing the classical biasing scheme studied in Section 4.5. The input signal v_{sig} is coupled to the gate through a very large capacitor (shown as infinite). The transistor source is connected to ground at signal frequencies via a very large capacitor (shown as infinite). The output voltage signal that develops at the drain is coupled to a load resistance via a very large capacitor (shown as infinite).

(a) If the transistor has $V_t = 1$ V, and $k'_n W/L = 2$ mA/V^2, verify that the bias circuit establishes $V_{GS} = 2$ V, $I_D = 1$ mA, and $V_D = +7.5$ V. That is, assume these values, and verify that they are consistent with the values of the circuit components and the device parameters.
(b) Find g_m and r_o if $V_A = 100$ V.
(c) Draw a complete small-signal equivalent circuit for the amplifier assuming all capacitors behave as short circuits at signal frequencies.
(d) Find R_{in}, v_{gs}/v_{sig}, v_o/v_{gs}, and v_o/v_{sig}.

4.78 The fundamental relationship that describes MOSFET operation is the parabolic relationship between V_{OV} and i_D,

$$i_D = \frac{1}{2} k'_n \frac{W}{L} v_{OV}^2$$

Sketch this parabolic curve together with the tangent at a point whose coordinates are (V_{OV}, I_D). The slope of this tangent is g_m at this bias point. Show that this tangent intersects the v_{OV}-axis at $V_{OV}/2$ and thus that $g_m = 2I_D/V_{OV}$.

SECTION 4.7: SINGLE-STAGE MOS AMPLIFIERS

4.79 Calculate the overall voltage gain G_v of a common-source amplifier for which $g_m = 2$ mA/V, $r_o = 50$ kΩ, $R_D = 10$ kΩ, and $R_G = 10$ MΩ. The amplifier is fed from a signal source with a Thévenin resistance of 0.5 MΩ, and the amplifier output is coupled to a load resistance of 20 kΩ.

D4.80 This problem investigates a redesign of the common-source amplifier of Exercise 4.32 whose bias design was done in Exercise 4.30 and shown in Fig. E4.30. Please refer to these two exercises.

(a) The open-circuit voltage gain of the CS amplifier can be written as

$$A_{vo} = -\frac{2(V_{DD} - V_D)}{V_{OV}}$$

Verify that this expression yields the results in Exercise 4.32 (i.e., $A_{vo} = -15$ V/V).
(b) A_{vo} can be doubled by reducing V_{OV} by a factor of 2, (i.e., from 1 V to 0.5 V) while V_D is kept unchanged. What corresponding values for I_D, R_D, g_m, and r_o apply?
(c) Find A_{vo} and R_{out} with r_{o1} taken into account.
(d) For the same value of signal-generator resistance $R_{sig} = 100$ kΩ, the same value of gate-bias resistance $R_G = 4.8$ MΩ, and the same value of load resistance $R_L = 15$ kΩ, evaluate the new value of overall voltage gain G_v with r_o taken into account.
(e) Compare your results to those obtained in Exercises 4.30 and 4.32, and comment.

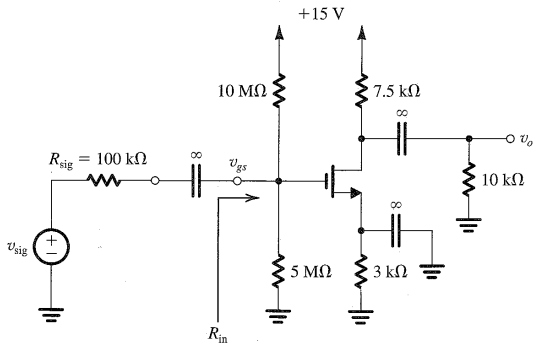

FIGURE P4.77

4.81 A common-gate amplifier using an n-channel enhancement MOS transistor for which $g_m = 5$ mA/V has a 5-kΩ drain resistance (R_D) and a 2-kΩ load resistance (R_L). The amplifier is driven by a voltage source having a 200-Ω resistance. What is the input resistance of the amplifier? What is the overall voltage gain G_v? If the circuit allows a bias-current increase by a factor of 4 while maintaining linear operation, what do the input resistance and voltage gain become?

4.82 A CS amplifier using an NMOS transistor biased in the manner of Fig. 4.43 for which $g_m = 2$ mA/V is found to have an overall voltage gain G_v of −16 V/V. What value should a resistance R_S inserted in the source lead have to reduce the voltage gain by a factor of 4?

4.83 The overall voltage gain of the amplifier of Fig. 4.44(a) was measured with a resistance R_S of 1 kΩ in place and found to be −10 V/V. When R_S is shorted, but the circuit operation remained linear the gain doubled. What must g_m be? What value of R_S is needed to obtain an overall voltage gain of −8 V/V?

4.84 Careful measurements performed on the source follower of Fig. 4.46(a) show that the open-circuit voltage gain is 0.98 V/V. Also, when R_L is connected and its value is varied, it is found that the gain is halved for $R_L = 500\ \Omega$. If the amplifier remained linear throughout this measurement, what must the values of g_m and r_o be?

4.85 The source follower of Fig. 4.46(a) uses a MOSFET biased to have $g_m = 5$ mA/V and $r_o = 20$ kΩ. Find the open-circuit voltage gain A_{vo} and the output resistance. What will the gain become when a 1-kΩ load resistance (R_L) is connected?

4.86 Figure P4.86 shows a scheme for coupling and amplifying a high-frequency pulse signal. The circuit utilizes two MOSFETs whose bias details are not shown and a 50-Ω coaxial cable. Transistor Q_1 operates as a CS amplifier and Q_2 as a CG amplifier. For proper operation, transistor Q_2 is required to present a 50-Ω resistance to the cable. This situation is known as "proper termination" of the cable and ensures that there will be no signal reflection coming back on the cable. When the cable is properly terminated, its input resistance is 50 Ω. What must g_{m2} be? If Q_1 is biased at the same point as Q_2, what is the amplitude of the current pulses in the drain of Q_1? What is the amplitude of the voltage pulses at the drain of Q_1? What value of R_D is required to provide 1-V pulses at the drain of Q_2?

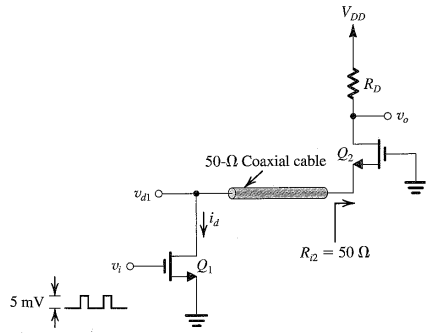

FIGURE P4.86

***D4.87** The MOSFET in the circuit of Fig. P4.87 has $V_t = 1$ V, $k'_n W/L = 0.8$ mA/V^2, and $V_A = 40$ V.

(a) Find the values of R_S, R_D, and R_G so that $I_D = 0.1$ mA, the largest possible value for R_D is used while a maximum signal swing at the drain of ±1 V is possible, and the input resistance at the gate is 10 MΩ.
(b) Find the values of g_m and r_o at the bias point.
(c) If terminal Z is grounded, terminal X is connected to a signal source having a resistance of 1 MΩ, and terminal Y is connected to a load resistance of 40 kΩ, find the voltage gain from signal source to load.
(d) If terminal Y is grounded, find the voltage gain from X to Z with Z open-circuited. What is the output resistance of the source follower?
(e) If terminal X is grounded and terminal Z is connected to a current source delivering a signal current of 10 μA and having a resistance of 100 kΩ, find the voltage signal that can be measured at Y. For simplicity, neglect the effect of r_o.

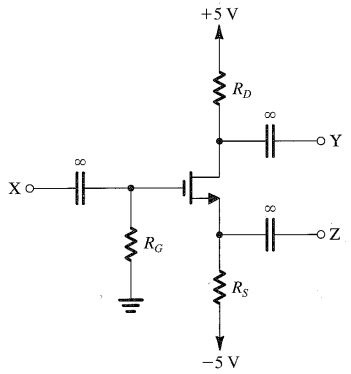

FIGURE P4.87

***4.88** (a) The NMOS transistor in the source-follower circuit of Fig. P4.88(a) has $g_m = 5$ mA/V and a large r_o. Find the open-circuit voltage gain and the output resistance.

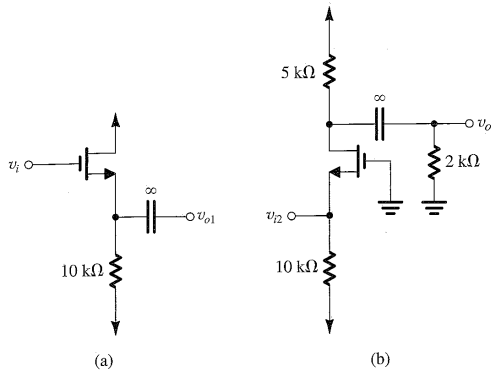

FIGURE P4.88

(b) The NMOS transistor in the common-gate amplifier of Fig. P4.88(b) has $g_m = 5$ mA/V and a large r_o. Find the input resistance and the voltage gain.
(c) If the output of the source follower in (a) is connected to the input of the common-gate amplifier in (b), use the results of (a) and (b) to obtain the overall voltage gain v_o/v_i.

***4.89** In this problem we investigate the large-signal operation of the source follower of Fig. 4.46(a). Specifically, consider the situation when negative input signals are applied. Let the negative signal voltage at the output be $-V$. The current in R_L will flow away from ground and will have a value of V/R_L. This current will subtract from the bias current I, resulting in a transistor current of $(I - V/R_L)$. One can use this current value to determine v_{GS}. Now the signal at the transistor source terminal will be $-V$, superimposed on the dc voltage, which is $-V_{GS}$ (corresponding to a drain current of I). We can thus find the signal voltage at the gate v_i. For the circuit analyzed in Exercise 4.34, find v_i for $v_o = -1$ V, -5 V, -6 V, and -7 V. At each point find the voltage gain v_o/v_i and compare to the small-signal value found in Exercise 4.34. What is the largest possible negative-output signal?

SECTION 4.8: THE MOSFET INTERNAL CAPACITANCES AND HIGH-FREQUENCY MODEL

4.90 Refer to the MOSFET high-frequency model in Fig. 4.47(a). Evaluate the model parameters for an NMOS transistor operating at $I_D = 100\ \mu$A, $V_{SB} = 1$ V, and $V_{DS} = 1.5$ V. The MOSFET has $W = 20\ \mu$m, $L = 1\ \mu$m, $t_{ox} = 8$ nm, $\mu_n = 450$ cm^2/Vs, $\gamma = 0.5$ V$^{1/2}$, $2\phi_f = 0.65$ V, $\lambda = 0.05$ V^{-1}, $V_0 = 0.7$ V, $C_{sb0} = C_{db0} = 15$ fF, and $L_{ov} = 0.05\ \mu$m. (Recall that $g_{mb} = \chi g_m$, where $\chi = \gamma/(2\sqrt{2\phi_f + V_{SB}})$.)

4.91 Find f_T for a MOSFET operating at $I_D = 100\ \mu$A and $V_{OV} = 0.25$ V. The MOSFET has $C_{gs} = 20$ fF and $C_{gd} = 5$ fF.

4.92 Starting from the definition of f_T for a MOSFET,

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

and making the approximation that $C_{gs} \gg C_{gd}$ and that the overlap component of C_{gs} is negligibly small, show that

$$f_T \simeq \frac{1.5}{\pi L}\sqrt{\frac{\mu_n I_D}{2C_{ox}WL}}$$

Thus note that to obtain a high f_T from a given device it must be operated at a high current. Also note that faster operation is obtained from smaller devices.

4.93 Starting from the expression for the MOSFET unity-gain frequency,

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

and making the approximation that $C_{gs} \gg C_{gd}$ and that the overlap component of C_{gs} is negligibly small, show that for an n-channel device

$$f_T = \frac{3\mu_n V_{OV}}{4\pi L^2}$$

Observe that for a given device, f_T can be increased by operating the MOSFET at a higher overdrive voltage. Evaluate f_T for devices with $L = 1.0\ \mu$m operated at overdrive voltages of 0.25 V and 0.5 V. Use $\mu_n = 450$ cm^2/Vs.

SECTION 4.9: FREQUENCY RESPONSE OF THE CS AMPLIFIER

4.94 In a particular MOSFET amplifier for which the midband voltage gain between gate and drain is -27 V/V, the NMOS transistor has $C_{gs} = 0.3$ pF and $C_{gd} = 0.1$ pF. What input capacitance would you expect? For what range of signal-source resistances can you expect the 3-dB frequency to exceed 10 MHz? Neglect the effect of R_G.

D4.95 In a FET amplifier, such as that in Fig. 4.49(a), the resistance of the source $R_{sig} = 100$ kΩ, amplifier input resistance (which is due to the biasing network) $R_{in} = 100$ kΩ, $C_{gs} = 1$ pF, $C_{gd} = 0.2$ pF, $g_m = 3$ mA/V, $r_o = 50$ kΩ, $R_D = 8$ kΩ, and $R_L = 10$ kΩ. Determine the expected 3-dB cutoff frequency f_H and the midband gain. In evaluating ways to double f_H, a designer considers the alternatives of changing either R_{out} or R_{in}. To raise f_H as described, what separate change in each would be required? What midband voltage gain results in each case?

4.96 A discrete MOSFET common-source amplifier has $R_{in} = 2$ MΩ, $g_m = 4$ mA/V, $r_o = 100$ kΩ, $R_D = 10$ kΩ, $C_{gs} = 2$ pF, and $C_{gd} = 0.5$ pF. The amplifier is fed from a voltage source with an internal resistance of 500 kΩ and is connected to a 10-kΩ load. Find:

(a) the overall midband gain A_M
(b) the upper 3-dB frequency f_H

4.97 The analysis of the high-frequency response of the common-source amplifier, presented in the text, is based on the assumption that the resistance of the signal source, R_{sig}, is large and, thus, that its interaction with the input capacitance C_{in} produces the "dominant pole" that determines the upper 3-dB frequency f_H. There are situations, however, when the CS amplifier is fed with a very low R_{sig}. To investigate the high-frequency response of the amplifier in such a case, Fig. P4.97 shows the equivalent circuit when the CS amplifier is fed with an ideal voltage source V_{sig} having $R_{sig} = 0$. Note that C_L denotes the total capacitance at the output node. By writing a node equation at the output, show that the transfer function V_o/V_{sig} is given by

$$\frac{V_o}{V_{sig}} = -g_m R_L' \frac{1 - s(C_{gd}/g_m)}{1 + s(C_L + C_{gd})R_L'}$$

At frequencies $\omega \ll (g_m/C_{gd})$, the s term in the numerator can be neglected. In such case, what is the upper 3-dB frequency resulting? Compute the values of A_M and f_H for the case: $C_{gd} = 0.5$ pF, $C_L = 2$ pF, $g_m = 4$ mA/V, and $R_L' = 5$ kΩ.

D4.98 Consider the common-source amplifier of Fig. 4.49(a). For a situation in which $R_{sig} = 1$ MΩ and $R_G = 1$ MΩ, what value of C_{C1} must be chosen to place the corresponding break frequency at 10 Hz? What value would you choose if available capacitors are specified to only one significant digit and the break frequency is not to exceed 10 Hz? What is the break frequency, f_{P1}, obtained with your choice? If a designer wishes to lower this by raising R_G, what is the most that he or she can expect if available resistors are limited to 10 times those now used?

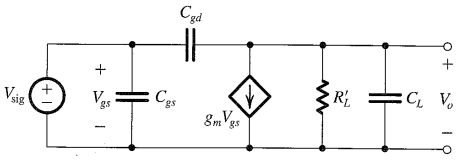

FIGURE P4.97

D4.99 The amplifier in Fig. P4.99 is biased to operate at $I_D = 1$ mA and $g_m = 1$ mA/V. Neglecting r_o, find the midband gain. Find the value of C_S that places f_L at 10 Hz.

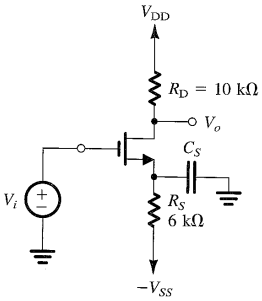

FIGURE P4.99

4.100 Consider the amplifier of Fig. 4.49(a). Let $R_D = 15$ kΩ, $r_o = 150$ kΩ, and $R_L = 10$ kΩ. Find the value of C_{C2}, specified to one significant digit, to ensure that the associated break frequency is at, or below, 10 Hz. If a higher-power design results in doubling I_D, with both R_D and r_o reduced by a factor of 2, what does the corner frequency (due to C_{C2}) become? For increasingly higher-power designs, what is the highest corner frequency that can be associated with C_{C2}.

4.101 The NMOS transistor in the discrete CS amplifier circuit of Fig. P4.101 is biased to have $g_m = 1$ mA/V. Find A_M, f_{P1}, f_{P2}, f_{P3}, and f_L.