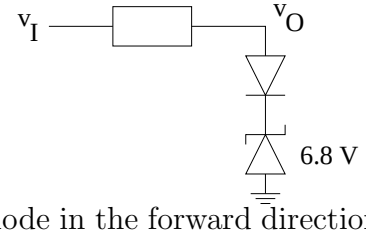
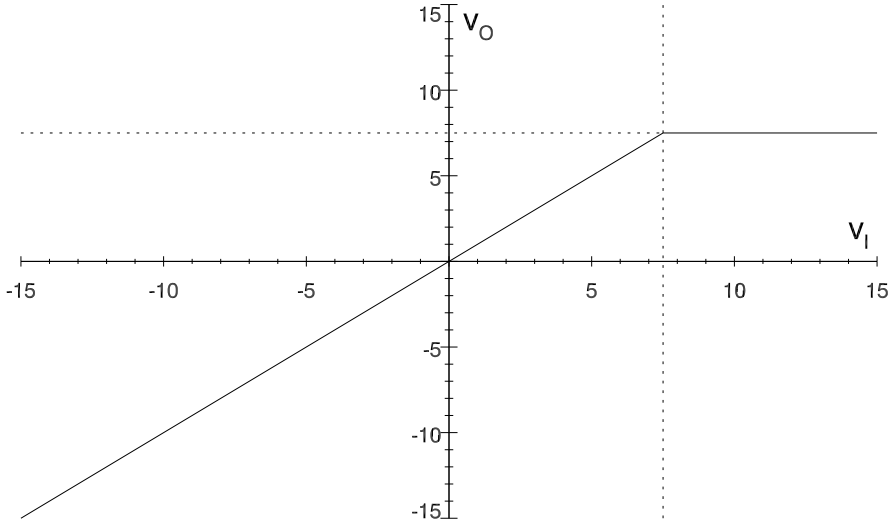
EE 321 Analog Electronics, Fall 2010
Exam 2 October 27, 2010
solution

Rules: This is a closed-book exam. You may use one small note card previously prepared. The exam will last 50 minutes. Each problem counts equally toward your grade. Skim all problems and begin with the ones that you find easiest. I have arranged the problems approximately such that the first ones require the least amount of math, and the last ones the most. No question requires more than a few lines of calculations.

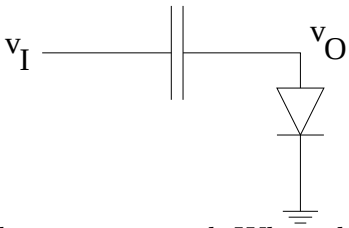
1. Limiter circuit. Sketch and clearly label the transfer characteristic (v_O as a function of v_I) for $-15\,\mathrm{V} < v_I < 15\,\mathrm{V}$ for this circuit. You may assume fixed $V_D = 0.7\,\mathrm{V}$, and $V_z = 6.8\,\mathrm{V}$ when conducting.



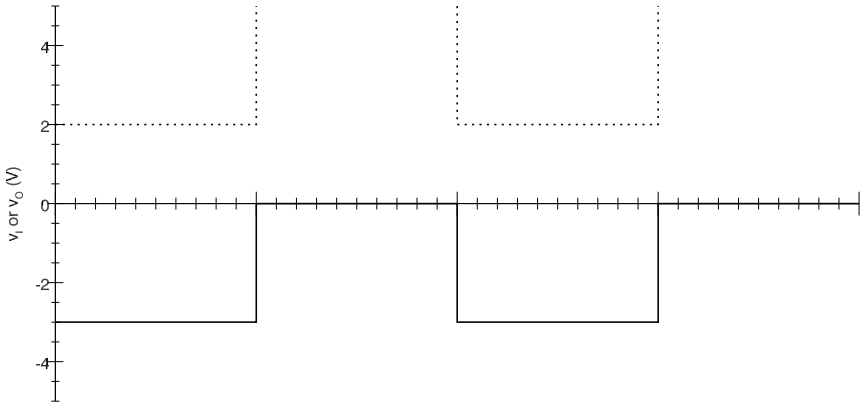
When $v_I > v_D + v_Z$, both diodes are conducting, the junction diode in the forward direction and the zener diode in the reverse breakdown region, and the output voltage equals the combined voltage drop, $v_O = v_D + v_Z = 0.7 + 6.8 = 7.5\,\mathrm{V}$. For any voltage less than that there is no conduction and thus $v_O = v_I$. Plotted it looks like this



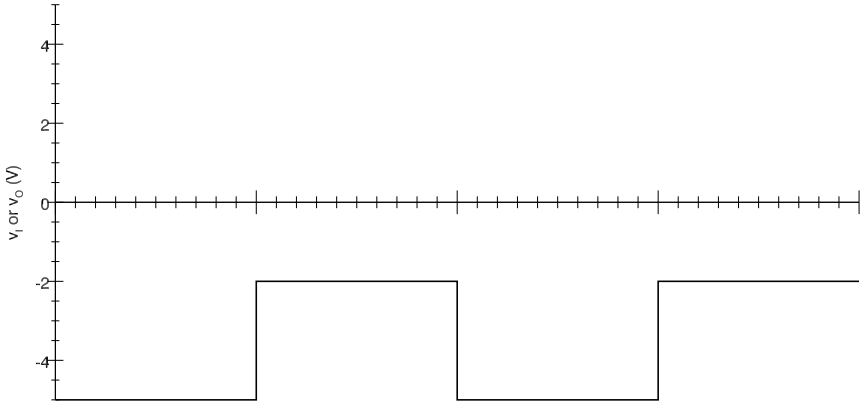
2. Clamped capacitor circuit. For the circuit below, sketch and clearly label the output when the input is (a) a square wave between 2 V and 5 V, and (b) a square wave between $-2\,\mathrm{V}$ and $-5\,\mathrm{V}$. You may assume the forward voltage drop across the diode is $V_D = 0\,\mathrm{V}$.



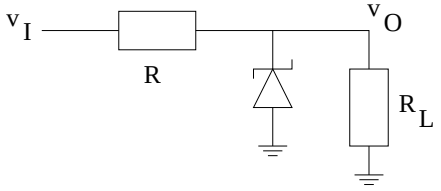
Current will flow from capacitor to ground when $v_I > 0$ until v_O becomes ground. When the voltage v_I is the lowered no current flows back. The result is that the waveform is shifted such that the maximum input voltage will correspond to ground on the output, if the maximum voltage is above ground. Thus for (a) we get (dotted is v_I and solid is v_O)



and for (b) we get the input and output to be equal,



3. Zener regulator. Consider this zener diode regulator circuit. $R = 1\,\mathrm{k\Omega}$ and $v_{Z0} = 6.8\,\mathrm{V}$. If the input is $v_I = 10\,\mathrm{V}$, at what maximum load current does regulation stop? What minimum load resistance does that correspond to? If $r_z = 10\,\Omega$, what is the regulation for zero load current (i.e. $R_L \to \infty$)?



The load current at which regulation stops corresponds to zero current through the zener diode. That would mean the following current through the load.

$$I = \frac{v_I - V_{Z0}}{R} = \frac{10 - 6.8}{1000} = 3.2\,\mathrm{mA}$$

The load resistance which causes that current to flow is

$$R_L = \frac{V_{Z0}}{I} = 2125\,\Omega$$

The regulation is $\frac{dv_O}{dv_I}$. So let's get v_O as af function of v_I.

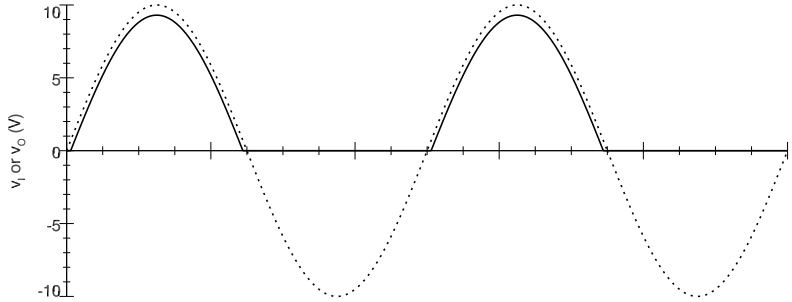
$$v_O = V_{Z0} + (v_I - V_{Z0})\,\frac{r_z}{R + r_z}$$

and then

$$\frac{dv_O}{dv_I} = \frac{r_z}{R + r_z} = \frac{10}{1000 + 10} = 0.01$$

4. Half-wave rectifier. For a half-wave rectifier, if the input is a sinusoid of amplitude $V_i = 10\,\mathrm{V}$, sketch the output and label the maximum output voltage. The frequency of the source is 100 Hz, and the load is 10 kΩ. Show where to add a capacitor to smooth the output. What size capacitor should be used to make the output ripple 1% of the peak output?

Here is first the input (dotted) and the output (solid) plotted together. The output is 0.7 V less than the input, but not less than zero. The maximum value of the output is $V_O = 9.3\,\mathrm{V}$.



The capacitor is placed in parallel with the load resistor. Next we get an expression for the size of the ripple. We linearly extrapolate the slope at the beginning of the exponential decay. As a function of time the decaying voltage is

$$v_O = V_O e^{-\frac{t}{RC}}$$

and the slop at the beginning of the day, $t = 0$, is

$$\left.\frac{dv_O}{dt}\right|_{t=0} = -\frac{V_O}{RC}$$

The voltage decays for approximately one period before the capacitor is recharged, so we have

$$\Delta V = \frac{V_O T}{RC}$$

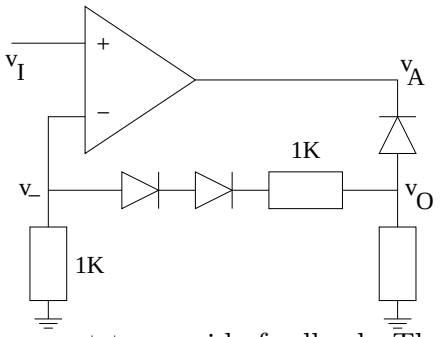
or

$$C = \frac{V_O T}{R\Delta V}$$

If $T = \frac{1}{f} = \frac{1}{100} = 0.01\,\mathrm{s}$, and $\frac{V_O}{\Delta V} = 100$, we get

$$C = \frac{V_O T}{R\Delta V} = \frac{100 \times 0.01}{10 \times 10^3} = 10^{-4}\,\mathrm{F} = 100\,\mu\mathrm{F}$$

5. Junction diode circuit. For this circuit determine v_A, v_O, and v_- for (a) $v_I = 2\,\mathrm{V}$, and (b) $v_I = -2\,\mathrm{V}$. Model the diodes as a fixed 0.7 V forward voltage drop when conducting. The op-amp saturates at $\pm 10\,\mathrm{V}$.



In case (a) when $v_I = 2\,\mathrm{V}$, the op-amp must be supplying current to provide feedback. That cannot happen because of the diodes, so the op-amp will saturate the output and no current will flow in the rest of the circuit. Thus, $v_A = 10\,\mathrm{V}$ and $v_O = v_- = 0\,\mathrm{V}$.

In case (b) the op-amp will attempt to sink current, which is possible, to balance the inputs. Thus, we know that $v_- = -2\,\mathrm{V}$. In that case v_O is two diode voltage drops and another 2 V drop across the $1\,\mathrm{k}\Omega$ resistor, so we get

$$v_O = v_- - V_D - V_D + v_- = -4 - 1.4 = -5.4\,\mathrm{V}$$

v_A is another diode voltage drop below v_O, so we get $v_A = -5.4 - 0.7 = -6.1\,\mathrm{V}$.