negative-output signal swing as determined by the need to keep the transistor in the active region. Present your results in a table.

D5.56 Consider the CE amplifier circuit of Fig. 5.26(a) when operated with a dc supply $V_{CC} = +5$ V. It is required to find the point at which the transistor should be biased; that is, find the value of V_{CE} so that the output sine-wave signal v_{ce} resulting from an input sine-wave signal v_{be} of 5-mV peak amplitude has the maximum possible magnitude. What is the peak amplitude of the output sine wave and the value of the gain obtained? Assume linear operation around the bias point. (*Hint:* To obtain the maximum possible output amplitude for a given input, you need to bias the transistor as close to the edge of saturation as possible without entering saturation at any time, that is, without v_{CE} decreasing below 0.3 V.)

5.57 The transistor in the circuit of Fig. P5.57 is biased at a dc collector current of 0.5 mA. What is the voltage gain? (*Hint:* Use Thévenin theorem to convert the circuit to the form in Fig. 5.26a).

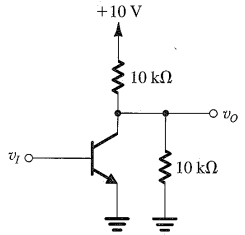

FIGURE P5.57

5.58 Sketch and label the voltage transfer characteristics of the *pnp* common-emitter amplifiers shown in Fig. P5.58.

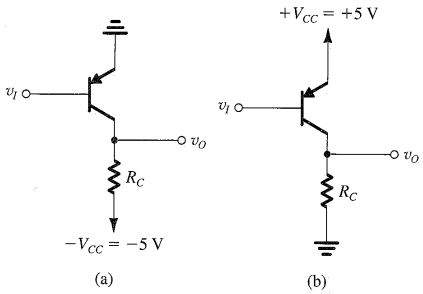

FIGURE P5.58

***5.59** In deriving the expression for small-signal voltage gain A_v in Eq. (5.56) we neglected the Early effect. Derive this expression including the Early effect, by substituting

$$i_C = I_S e^{v_{BE}/V_T}\left(1 + \frac{v_{CE}}{V_A}\right)$$

in Eq. (5.50). Show that the gain expression changes to

$$A_v = \frac{-I_C R_C/V_T}{\left[1 + \dfrac{I_C R_C}{V_A + V_{CE}}\right]} = -\frac{(V_{CC} - V_{CE})/V_T}{\left[1 + \dfrac{V_{CC} - V_{CE}}{V_A + V_{CE}}\right]}$$

For the case $V_{CC} = 5$ V and $V_{CE} = 2.5$ V, what is the gain without and with the Early effect taken into account? Let $V_A = 100$ V.

5.60 When the common-emitter amplifier circuit of Fig. 5.26(a) is biased with a certain V_{BE}, the dc voltage at the collector is found to be +2 V. For $V_{CC} = +5$ V and $R_C = 1$ kΩ, find I_C and the small-signal voltage gain. For a change $\Delta v_{BE} = +5$ mV, calculate the resulting Δv_O. Calculate it two ways: by finding Δi_C using the transistor exponential characteristic and approximately using the small-signal voltage gain. Repeat for $\Delta v_{BE} = -5$ mV. Summarize your results in a table.

***5.61** Consider the common-emitter amplifier circuit of Fig. 5.26(a) when operated with a supply voltage $V_{CC} = +5$ V.

(a) What is the theoretical maximum voltage gain that this amplifier can provide?
(b) What value of V_{CE} must this amplifier be biased at to provide a voltage gain of −100 V/V?
(c) If the dc collector current I_C at the bias point in (b) is to be 0.5 mA, what value of R_C should be used?
(d) What is the value of V_{BE} required to provide the bias point mentioned above? Assume that the BJT has $I_S = 10^{-15}$ A.
(e) If a sine-wave signal v_{be} having a 5-mV peak amplitude is superimposed on V_{BE}, find the corresponding output voltage signal v_{ce} that will be superimposed on V_{CE} assuming linear operation around the bias point.
(f) Characterize the signal current i_c that will be superimposed on the dc bias current I_C.
(g) What is the value of the dc base current I_B at the bias point. Assume $\beta = 100$. Characterize the signal current i_b that will be superimposed on the base current I_B.
(h) Dividing the amplitude of v_{be} by the amplitude of i_b, evaluate the incremental (or small-signal) input resistance of the amplifier.
(i) Sketch and clearly label correlated graphs for v_{BE}, v_{CE}, i_C, and i_B. Note that each graph consists of a dc or average value and a superimposed sine wave. Be careful of the phase relationships of the sine waves.

5.62 The essence of transistor operation is that a change in v_{BE}, Δv_{BE}, produces a change in i_C, Δi_C. By keeping Δv_{BE} small, Δi_C is approximately linearly related to Δv_{BE}, $\Delta i_C = g_m \Delta v_{BE}$, where g_m is known as the transistor transconductance. By passing Δi_C through R_C, an output voltage signal Δv_O is obtained. Use the expression for the small-signal voltage gain in Eq. (5.56) to derive an expression for g_m. Find the value of g_m for a transistor biased at $I_C = 1$ mA.

5.63 Consider the characteristic curves shown in Fig. 5.29 with the following additional calibration data: Label, from the lowest colored line, $i_B = 1$ μA, 10 μA, 20 μA, 30 μA, and 40 μA. Assume the lines to be horizontal, and let $\beta = 100$. For $V_{CC} = 5$ V and $R_C = 1$ kΩ, what peak-to-peak collector voltage swing will result for i_B varying over the range 10 μA to 40 μA? If, at a new bias point (not the one shown in the figure) $V_{CE} = \frac{1}{2}V_{CC}$, find the value of I_C and I_B. If at this current $V_{BE} = 0.7$ V and if $R_B = 100$ kΩ, find the required value of V_{BB}.

***5.64** Sketch the i_C–v_{CE} characteristics of an *npn* transistor having $\beta = 100$ and $V_A = 100$ V. Sketch characteristic curves for $i_B = 20$ μA, 50 μA, 80 μA, and 100 μA. For the purpose of this sketch, assume that $i_C = \beta i_B$ at $v_{CE} = 0$. Also, sketch the load line obtained for $V_{CC} = 10$ V and $R_C = 1$ kΩ. If the dc bias current into the base is 50 μA, write the equation for the corresponding i_C–v_{CE} curve. Also, write the equation for the load line, and solve the two equations to obtain V_{CE} and I_C. If the input signal causes a sinusoidal signal of 30-μA peak amplitude to be superimposed on I_B, find the corresponding signal components of i_C and v_{CE}.

D5.65 For the circuit in Fig. P5.65 select a value for R_B so that the transistor saturates with an overdrive factor of 10. The BJT is specified to have a minimum β of 20 and $V_{CEsat} = 0.2$ V. What is the value of forced β achieved?

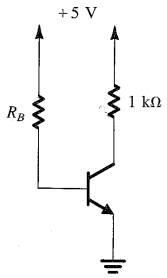

FIGURE P5.65

D5.66 For the circuit in Fig. P5.66 select a value for R_E so that the transistor saturates with a forced β of 10. Assume $V_{EB} = 0.7$ V and $V_{ECsat} = 0.2$ V.

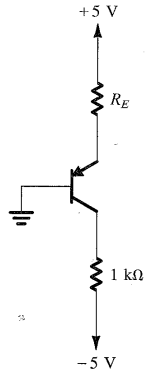

FIGURE P5.66

5.67 For each of the saturated circuits in Fig. P5.67, find i_B, i_C, and i_E. Use $|V_{BE}| = 0.7$ V and $|V_{CEsat}| = 0.2$ V.

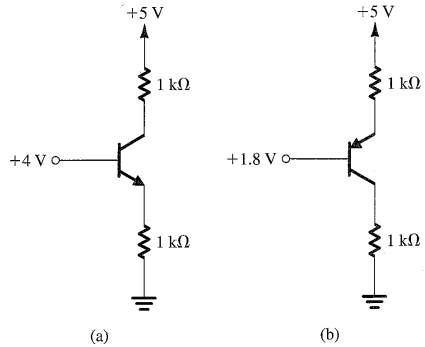

FIGURE P5.67

***5.68** Consider the operation of the circuit shown in Fig. P5.68 as v_B rises slowly from zero. For this transistor, assume $\beta = 50$, v_{BE} at which the transistor conducts is 0.5 V, v_{BE} when fully conducting is 0.7 V, saturation begins at $v_{BC} = 0.4$ V, and the transistor is deeply in saturation at $v_{BC} = 0.6$ V. Sketch and label v_E and v_C versus v_B. For what range of v_B is i_C essentially zero? What are the values of v_E, i_E, i_C, and v_C for $v_B = 1$ V and 3 V? For what value of v_B does saturation begin? What is i_B at this point? For $v_B = 4$ V and 6 V, what are the values of v_E, v_C, i_E, i_C, and i_B? Augment your sketch by adding a plot of i_B.