from which the common-mode gain can be obtained as

$$A_{cm} = \left(\frac{R_D}{2R_{SS}}\right)\left(\frac{\Delta g_m}{g_m}\right) \tag{7.64}$$

Since the g_m mismatch will have a negligible effect on A_d,

$$A_d \cong -g_m R_D \tag{7.65}$$

and the CMRR resulting will be

$$\text{CMRR} \equiv \left|\frac{A_d}{A_{cm}}\right| = (2g_m R_{SS})\Big/\left(\frac{\Delta g_m}{g_m}\right) \tag{7.66}$$

The similarity of this expression to that resulting from the R_D mismatch (Eq. 7.53) should be noted.

EXERCISE

7.6 For the MOS amplifier specified in Exercise 7.5 with the output taken differentially compute CMRR that results from a 1% mismatch in g_m.

Ans. 86 dB

7.3 THE BJT DIFFERENTIAL PAIR

Figure 7.12 shows the basic BJT differential-pair configuration. It is very similar to the MOSFET circuit and consists of two matched transistors, Q_1 and Q_2, whose emitters are joined together and biased by a constant-current source I. The latter is usually implemented by a transistor circuit of the type studied in Sections 6.3 and 6.12. Although each collector is shown connected to the positive supply voltage V_{CC} through a resistance R_C, this connection is not essential to the operation of the differential pair—that is, in some applications the two collectors may be connected to other transistors rather than to resistive loads. It is essential, though, that the collector circuits be such that Q_1 and Q_2 never enter saturation.

7.3.1 Basic Operation

To see how the BJT differential pair works, consider first the case of the two bases joined together and connected to a common-mode voltage v_{CM}. That is, as shown in Fig. 7.13(a),

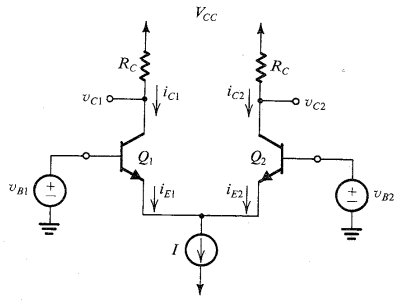

FIGURE 7.12 The basic BJT differential-pair configuration.

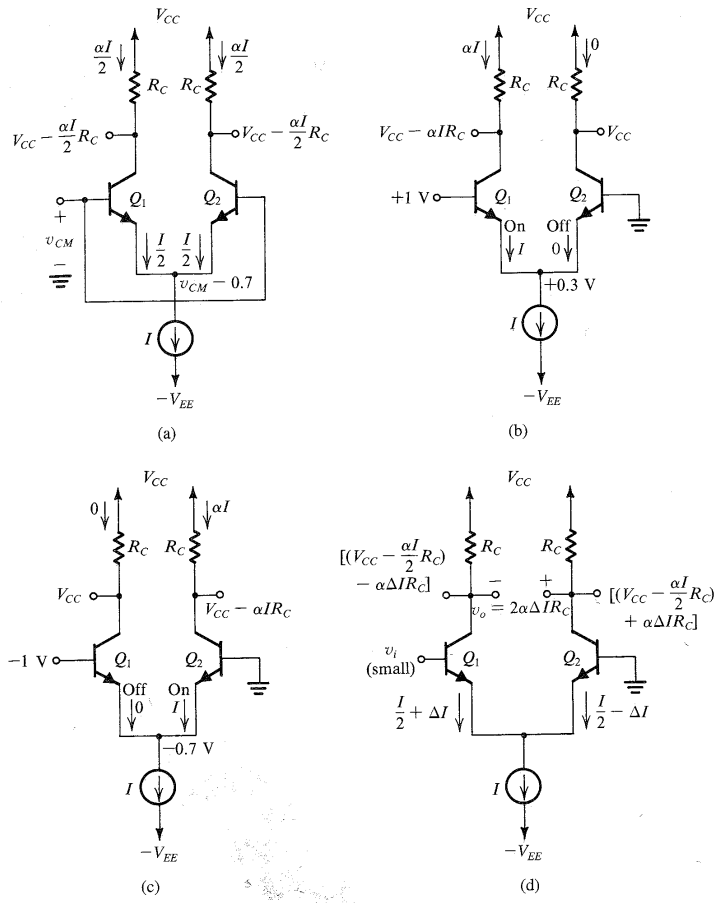

FIGURE 7.13 Different modes of operation of the BJT differential pair: **(a)** The differential pair with a common-mode input signal v_{CM}. **(b)** The differential pair with a "large" differential input signal. **(c)** The differential pair with a large differential input signal of polarity opposite to that in (b). **(d)** The differential pair with a small differential input signal v_i. Note that we have assumed the bias current source I to be ideal (i.e., it has an infinite output resistance) and thus I remains constant with the change in v_{CM}.

$v_{B1} = v_{B2} = v_{CM}$. Since Q_1 and Q_2 are matched, and assuming an ideal bias current source I with infinite output resistance, it follows that the current I will remain constant and from symmetry that I will divide equally between the two devices. Thus $i_{E1} = i_{E2} = I/2$, and the voltage at the emitters will be $v_{CM} - V_{BE}$, where V_{BE} is the base–emitter voltage (assumed in Fig 7.13a to be