of these situations? Now for $v_{G2} = 0$ V, at what voltages must v_{G1} be placed to reduce i_{D2} by 10%? to increase i_{D2} by 10%? What is the differential voltage, $v_{id} = v_{G2} - v_{G1}$, for which the ratio of drain currents i_{D2}/i_{D1} is 1.0? 0.5? 0.9? 0.99? For the current ratio $i_{D1}/i_{D2} = 20.0$, what differential input is required?

SECTION 7.2: SMALL-SIGNAL OPERATION OF THE MOS DIFFERENTIAL PAIR

7.11 An NMOS differential amplifier is operated at a bias current I of 0.5 mA and has a W/L ratio of 50, $\mu_n C_{ox} = 250\ \mu A/V^2$, $V_A = 10$ V, and $R_D = 4$ kΩ. Find V_{OV}, g_m, r_o, and A_d.

D7.12 It is required to design an NMOS differential amplifier to operate with a differential input voltage that can be as high as 0.2 V while keeping the nonlinear term under the square root in Eq. (7.23) to a maximum of 0.1. A transconductance g_m of 3 mA/V is needed. Find the required values of V_{OV}, I, and W/L. Assume that the technology available has $\mu_n C_{ox} = 100\ \mu A/V^2$. What differential gain A_d results when $R_D = 5$ kΩ? Assume $\lambda = 0$. What is the resulting output signal corresponding to v_{id} at its maximum value?

D*7.13 Figure P7.13 shows a circuit for a differential amplifier with an active load. Here Q_1 and Q_2 form the differential pair while the current source transistors Q_4 and Q_5 form the active loads for Q_1 and Q_2, respectively. The dc bias circuit that establishes an appropriate dc voltage at the drains of Q_1 and Q_2 is not shown. Note that the equivalent differential half-circuit is an active-loaded common-source transistor of the type studied in Section 6.5. It is required to design the circuit to meet the following specifications:

(a) Differential gain $A_d = 80$ V/V.
(b) $I_{REF} = I = 100\ \mu$A.
(c) The dc voltage at the gates of Q_6 and Q_3 is +1.5 V.
(d) The dc voltage at the gates of Q_7, Q_4, and Q_5 is −1.5 V.

The technology available is specified as follows: $\mu_n C_{ox} = 3\mu_p C_{ox} = 90\ \mu A/V^2$; $V_{tn} = |V_{tp}| = 0.7$ V, $V_{An} = |V_{Ap}| = 20$ V. Specify the required value of R and the W/L ratios for all transistors. Also specify I_D and $|V_{GS}|$ at which each transistor is operating. For dc bias calculations you may neglect channel-length modulation.

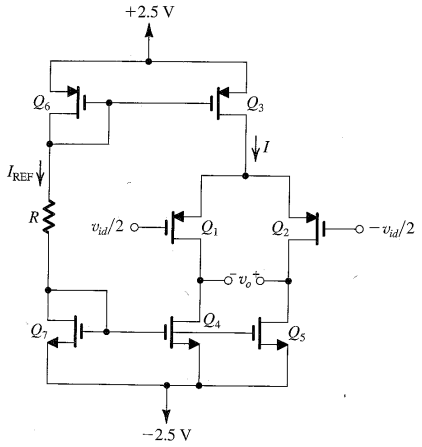

FIGURE P7.13

7.14 A design error has resulted in a gross mismatch in the circuit of Fig. P7.14. Specifically, Q_2 has twice the W/L ratio of Q_1. If v_{id} is a small sine-wave signal, find:

(a) I_{D1} and I_{D2}.
(b) V_{OV} for each of Q_1 and Q_2.
(c) The differential gain A_d in terms of R_D, I, and V_{OV}.

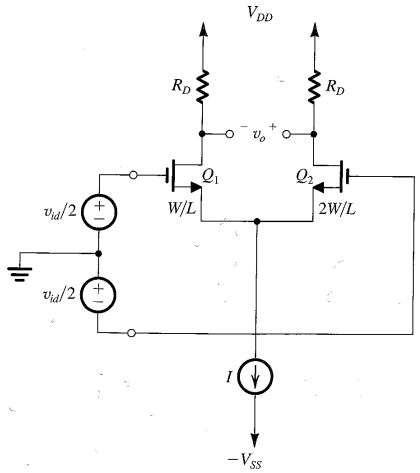

FIGURE P7.14

7.15 An NMOS differential pair is biased by a current source $I = 0.2$ mA having an output resistance $R_{SS} = 100$ kΩ. The amplifier has drain resistances $R_D = 10$ kΩ, using transistors with $k'_n W/L = 3\ mA/V^2$, and r_o that is large.

(a) If the output is taken single-endedly, find $|A_d|$, $|A_{cm}|$, and CMRR.
(b) If the output is taken differentially and there is a 1% mismatch between the drain resistances, find $|A_d|$, $|A_{cm}|$, and CMRR.

7.16 For the differential amplifier shown in Fig. P7.2, let Q_1 and Q_2 have $k'_p(W/L) = 3.5\ mA/V^2$, and assume that the bias current source has an output resistance of 30 kΩ. Find V_{OV}, g_m, $|A_d|$, $|A_{cm}|$, and the CMRR (in dB) obtained with the output taken differentially. The drain resistances are known to have a mismatch of 2%.

D*7.17 The differential amplifier in Fig. P7.17 utilizes a resistor R_{SS} to establish a 1-mA dc bias current. Note that this amplifier uses a single 5-V supply and thus needs a dc common-mode voltage V_{CM}. Transistors Q_1 and Q_2 have $k'_n W/L = 2.5\ mA/V^2$, $V_t = 0.7$ V, and $\lambda = 0$.

(a) Find the required value of V_{CM}.
(b) Find the value of R_D that results in a differential gain A_d of 8 V/V.
(c) Determine the dc voltage at the drains.
(d) Determine the common-mode gain $\Delta V_{D1}/\Delta V_{CM}$. (*Hint:* You need to take $1/g_m$ into account.)
(e) Use the common-mode gain found in (d) to determine the change in V_{CM} that results in Q_1 and Q_2 entering the triode region.

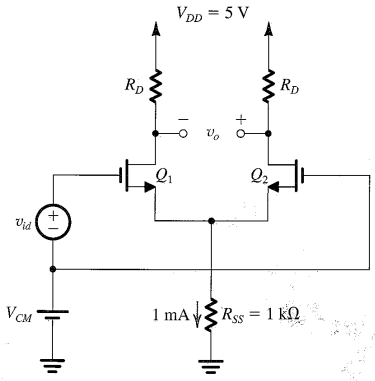

FIGURE P7.17

***7.18** The objective of this problem is to determine the common-mode gain and hence the CMRR of the differential pair arising from a simultaneous mismatch in g_m and in R_D.

(a) Refer to the circuit in Fig. 7.11 and let the two drain resistors be denoted R_{D1} and R_{D2} where $R_{D1} = R_D + (\Delta R_D/2)$ and $R_{D2} = R_D - (\Delta R_D/2)$. Also let $g_{m1} = g_m + (\Delta g_m/2)$ and $g_{m2} = g_m - (\Delta g_m/2)$. Follow an analysis process similar to that used to derive Eq. (7.64) to show that

$$A_{cm} \cong \left(\frac{R_D}{2R_{SS}}\right)\left(\frac{\Delta g_m}{g_m} + \frac{\Delta R_D}{R_D}\right)$$

Note that this equation indicates that R_D can be deliberately varied to compensate for the initial variability in g_m and R_D, that is, to minimize A_{cm}.
(b) In a MOS differential amplifier for which $R_D = 5$ kΩ and $R_{SS} = 25$ kΩ, the common-mode gain is measured and found to be 0.002 V/V. Find the percentage change required in one of the two drain resistors so as to reduce A_{cm} to zero (or close to zero).

7.19 Recalling that g_m of a MOSFET is given by

$$g_m = k'_n\left(\frac{W}{L}\right)(V_{GS} - V_t)$$

we observe that there are two potential sources for a mismatch between the g_m values in a differential pair: a mismatch $\Delta(W/L)$ in the (W/L) values and a mismatch ΔV_t in the threshold voltage values. Hence show that

$$\frac{\Delta g_m}{g_m} = \frac{\Delta(W/L)}{W/L} + \frac{\Delta V_t}{V_{OV}}$$

Evaluate the worst-case fractional mismatch in g_m for a differential pair in which the (W/L) values have a tolerance of ±1% and the largest mismatch in V_t is specified to be 5 mV. Assume that the pair is operating at $V_{OV} = 0.25$ V. If $R_D = 5$ kΩ and $R_{SS} = 25$ kΩ, find the worst-case value of A_{cm}. If the bias current $I = 1$ mA, find the corresponding worst-case CMRR.

SECTION 7.3: THE BJT DIFFERENTIAL PAIR

7.20 For the differential amplifier of Fig. 7.13(a) let $I = 1$ mA, $V_{CC} = 5$ V, $v_{CM} = -2$ V, $R_C = 3$ kΩ, and $\beta = 100$. Assume that the BJTs have $v_{BE} = 0.7$ V at $i_C = 1$ mA. Find the voltage at the emitters and at the outputs.

7.21 For the circuit of Fig. 7.13(b) with an input of +1 V as indicated, and with $I = 1$ mA, $V_{CC} = 5$ V, $R_C = 3$ kΩ, and $\beta = 100$, find the voltage at the emitters and the collector voltages. Assume that the BJTs have $v_{BE} = 0.7$ V at $i_C = 1$ mA.

7.22 Repeat Exercise 7.7 (page.X) for an input of −0.3 V.

7.23 For the BJT differential amplifier of Fig. 7.12 find the value of the input differential signal, $v_{id} \equiv v_{B1} - v_{B2}$, that causes $i_{E1} = 0.80I$.

D7.24 Consider the differential amplifier of Fig. 7.12 and let the BJT β be very large:

(a) What is the largest input common-mode signal that can be applied while the BJTs remain comfortably in the active region with $v_{CB} = 0$?

(b) If an input difference signal is applied that is large enough to steer the current entirely to one side of the pair, what is the change in voltage at each collector (from the condition for which $v_{id} = 0$)?
(c) If the available power supply V_{CC} is 5 V, what value of IR_C should you choose in order to allow a common-mode input signal of ±3 V?
(d) For the value of IR_C found in (c), select values for I and R_C. Use the largest possible value for I subject to the constraint that the base current of each transistor (when I divides equally) should not exceed 2 μA. Let $\beta = 100$.

7.25 To provide insight into the possibility of nonlinear distortion resulting from large differential input signals applied to the differential amplifier of Fig. 7.12, evaluate the normalized change in the current i_{E1}, $\Delta i_{E1}/I = (i_{E1} - (I/2))/I$, for differential input signals v_{id} of 5, 10, 20, 30, and 40 mV. Provide a tabulation of the ratio $((\Delta i_{E1}/I)/v_{id})$, which represents the proportional transconductance gain of the differential pair, versus v_{id}. Comment on the linearity of the differential pair as an amplifier.

D7.26 Design the circuit of Fig. 7.12 to provide a differential output voltage (i.e., one taken between the two collectors) of 1 V when the differential input signal is 10 mV. A current source of 2 mA and a positive supply of +10 V are available. What is the largest possible input common-mode voltage for which operation is as required? Assume $\alpha \simeq 1$.

D*7.27 One of the trade-offs available in the design of the basic differential amplifier circuit of Fig. 7.12 is between the value of the voltage gain and the range of common-mode input voltage. The purpose of this problem is to demonstrate this trade-off.

(a) Use Eqs. (7.72) and (7.73) to obtain i_{C1} and i_{C2} corresponding to a differential input signal of 5 mV (i.e., $v_{B1} - v_{B2} = 5$ mV). Assume β to be very high. Find the resulting voltage difference between the two collectors ($v_{C2} - v_{C1}$), and divide this value by 5 mV to obtain the voltage gain in terms of (IR_C).
(b) Find the maximum permitted value for v_{CM} (Fig. 7.13a) while the transistors remain comfortably in the active mode with $v_{CB} = 0$. Express this maximum in terms of V_{CC} and the gain, and hence show that for a given value of V_{CC}, the higher the gain achieved, the lower the common-mode range. Use this expression to find $v_{CM\max}$ corresponding to a gain magnitude of 100, 200, 300, and 400 V/V. For each value, also give the required value of IR_C and the value of R_C for $I = 1$ mA.

***7.28** For the circuit in Fig. 7.12, assuming $\alpha = 1$ and $IR_C = 5$ V, use Eqs. (7.67) and (7.68) to find i_{C1} and i_{C2}, and hence determine $v_o = v_{C2} - v_{C1}$ for input differential signals $v_{id} \equiv v_{B1} - v_{B2}$ of 5 mV, 10 mV, 15 mV, 20 mV, 25 mV, 30 mV, 35 mV, and 40 mV. Plot v_o versus v_{id}, and hence comment on the amplifier linearity. As another way of visualizing linearity, determine the gain (v_o/v_{id}) versus v_{id}. Comment on the resulting graph.

7.29 In a differential amplifier using a 6-mA emitter bias current source the two BJTs are not matched. Rather, one has one-and-a-half times the emitter junction area of the other. For a differential input signal of zero volts, what do the collector currents become? What difference input is needed to equalize the collector currents? Assume $\alpha = 1$.

***7.30** Figure P7.30 shows a logic inverter based on the differential pair. Here, Q_1 and Q_2 form the differential pair, whereas Q_3 is an emitter follower that performs two functions: It shifts the level of the output voltage to make V_{OH} and V_{OL} centered on the reference voltage V_R, thus enabling one gate to drive another (this point will be explained in detail in Chapter 11), and it provides the inverter with a low output resistance. All transistors have $V_{BE} = 0.7$ V at $I_C = 1$ mA and have $\beta = 100$.

(a) For v_I sufficiently low that Q_1 is cut off, find the value of the output voltage v_O. This is V_{OH}.
(b) For v_I sufficiently high that Q_1 is carrying all the current I, find the output voltage v_O. This is V_{OL}.
(c) Determine the value of v_I that results in Q_1 conducting 1% of I. This can be taken as V_{IL}.
(d) Determine the value of v_I that results in Q_1 conducting 99% of I. This can be taken as V_{IH}.
(e) Sketch and clearly label the breakpoints of the inverter voltage transfer characteristic. Calculate the values of the noise margins NM_H and NM_L. Note the judicious choice of the value of the reference voltage V_R.

(For the definitions of the parameters that are used to characterize the inverter VTC, refer to Section 1.7.)

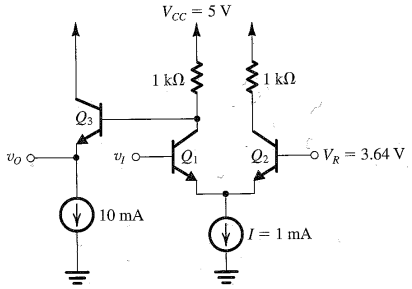

FIGURE P7.30

7.31 A BJT differential amplifier uses a 300-μA bias current. What is the value of g_m of each device? If β is 150, what is the differential input resistance?

D7.32 Design the basic BJT differential amplifier circuit of Fig. 7.16 to provide a differential input resistance of at least 10 kΩ and a differential voltage gain (with the output taken between the two collectors) of 200 V/V. The transistor β is specified to be at least 100. The available power supply is 10 V.

7.33 For a differential amplifier to which a total difference signal of 10 mV is applied, what is the equivalent signal to its corresponding CE half-circuit? If the emitter current source is 100 μA, what is r_e of the half-circuit? For a load resistance of 10 kΩ in each collector, what is the half-circuit gain? What magnitude of signal output voltage would you expect at each collector?

7.34 A BJT differential amplifier is biased from a 2-mA constant-current source and includes a 100-Ω resistor in each emitter. The collectors are connected to V_{CC} via 5-kΩ resistors. A differential input signal of 0.1 V is applied between the two bases.

(a) Find the signal current in the emitters (i_e) and the signal voltage v_{be} for each BJT.
(b) What is the total emitter current in each BJT?
(c) What is the signal voltage at each collector? Assume $\alpha = 1$.
(d) What is the voltage gain realized when the output is taken between the two collectors?

D7.35 Design a BJT differential amplifier to amplify a differential input signal of 0.2 V and provide a differential output signal of 4 V. To ensure adequate linearity, it is required to limit the signal amplitude across each base–emitter junction to a maximum of 5 mV. Another design requirement is that the differential input resistance be at least 80 kΩ. The BJTs available are specified to have $\beta \geq 200$. Give the circuit configuration and specify the values of all its components.

7.36 A particular differential amplifier operates from an emitter current source whose output resistance is 1 MΩ. What resistance is associated with each common-mode half-circuit? For collector resistors of 20 kΩ, what is the resulting common-mode gain for output taken (a) differentially, (b) single-endedly?

7.37 Find the voltage gain and the input resistance of the amplifier shown in Fig. P7.37 assuming $\beta = 100$.

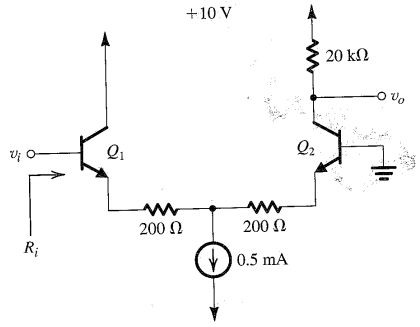

FIGURE P7.37

7.38 Find the voltage gain and input resistance of the amplifier in Fig. P7.38 assuming that $\beta = 100$.

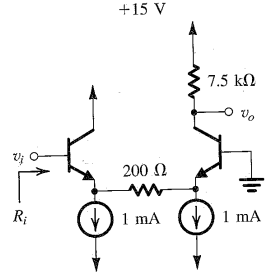

FIGURE P7.38

7.39 Derive an expression for the small-signal voltage gain v_o/v_i of the circuit shown in Fig. P7.39 in two different ways:

(a) as a differential amplifier
(b) as a cascade of a common-collector stage Q_1 and a common-base stage Q_2

Assume that the BJTs are matched and have a current gain α. Verify that both approaches lead to the same result.

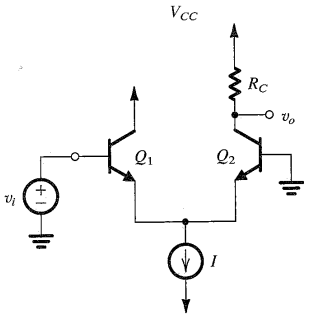

FIGURE P7.39

7.40 The differential amplifier circuit of Fig. P7.40 utilizes a resistor connected to the negative power supply to establish the bias current I.

(a) For $v_{B1} = v_{id}/2$ and $v_{B2} = -v_{id}/2$, where v_{id} is a small signal with zero average, find the magnitude of the differential gain, $|v_o/v_{id}|$.
(b) For $v_{B1} = v_{B2} = v_{icm}$, find the magnitude of the common-mode gain, $|v_o/v_{icm}|$.
(c) Calculate the CMRR.