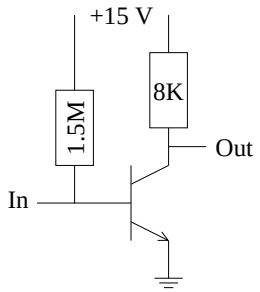
EE 321 Analog Electronics, Fall 2010
Exam 3 November 17, 2010

Rules: This is a closed-book exam. You may use one small note card previously prepared and the attached formula sheet. The exam will last 50 minutes. Each problem counts equally toward your grade. **IMPORTANT: Use symbolic math or loose points: name the resistors and voltages using the usual terminology and only insert numerical values at the end**.

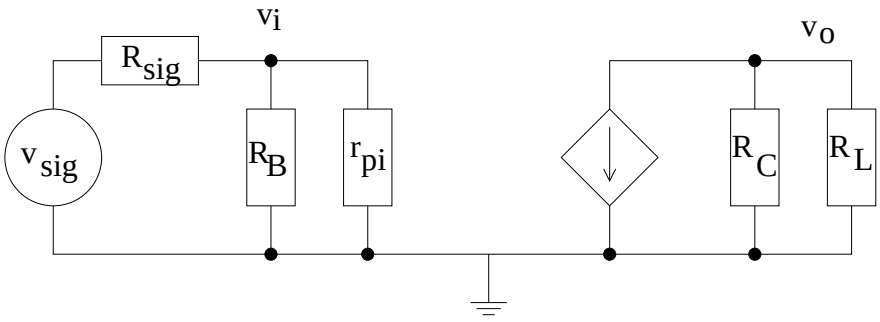
1. NPN Single-stage amplifier. For this circuit give the three terminal voltages and the three terminal currents. Assume $\beta = 100$. Draw a small-signal model. What is the gain A_{vo}? If a signal, v_{sig}, with output resistance 1 kΩ is attached to the input and a 10 kΩ resistor is attached to the output, what is the overall gain, v_o/v_{sig}?



Terminal voltages and currents:
It is easy to see that $V_E = 0$ and $V_B = V_{BE} = 0.7\,\text{V}$.

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{15 - 0.7}{1.5} = 9.5\,\mu\text{A}$$

Then, assuming active mode, $I_C = \beta I_B = 0.95\,\text{mA}$ and $I_E = 0.96\,\text{mA}$. $V_C = V_{CC} - I_C R_C = 15 - 8 \times 0.96 = 7.37\,\text{V}$.
Small-signal model:



Including the signal generator and load resistor.
Open-circuit gain A_{vo}:

$$A_{vo} = -g_m R_c = -0.0384 \times 8 \times 10^3 = -307$$

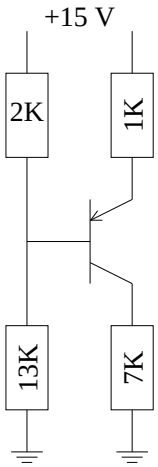
where $g_m = \frac{I_C}{V_T} = \frac{0.96}{25} = 0.0384\,\Omega^{-1}$
Gain, G_v:

$$G_v = -\frac{R_B||r_\pi}{R_{\text{sig}} + R_B||r_\pi} g_m \left(R_C||R_L\right)$$

where $r_\pi = \frac{\beta}{g_m} = \frac{100}{0.0384} = 2.6\,\text{k}\Omega$, and $R_B||r_\pi = 2.6\,\text{k}\Omega$. Then

$$G_v = -\frac{2.6}{1+2.6} \times 0.0384 \times (8||10) \times 10^3 = 123$$

2. PNP single-stage amplifier. For this circuit give the three terminal voltages and the three terminal currents. Assume $\beta = 100$. What is the gain A_{vo}? If a signal, v_{sig}, with output resistance 1 kΩ is attached to the input, and the output is open, what is the overall voltage gain, v_o/v_{sig}? Use quick approximations for both gain and input resistance or you will run out of time.



The current into the base is small compared to the current in the base biase voltage divider so we ignore the base current and get

$$V_B = V_{CC}\frac{R_2}{R_1+R_2} = 15 \times \frac{13}{2+13} = 13\,\text{V}$$

Then $V_E = V_B + V_{EB} = 13 + 0.7 = 13.7\,\text{V}$. Then

$$I_E = \frac{V_{CC} - V_E}{R_E} = \frac{15 - 13.7}{1} = 1.3\,\text{mA}$$

Then $I_B = \frac{I_E}{\beta+1} = \frac{1.3}{101} = 13\,\mu\text{A}$ and $I_C = \alpha \underset{=}{\frac{I_E}{}} \frac{100}{101} \times 1.3 = 1.29\,\text{mA}$, and then

$$V_E = I_E R_E = 1.29 \times 7 = 9\,\text{V}$$

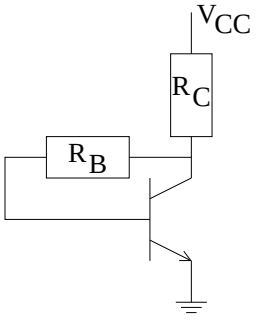
The open-circuit gain is

$$A_{vo} = -\frac{R_C}{R_E} = -\frac{7}{1} = -7$$

The overall gain is A_{vo} multiplied by the voltage division between the input and signal resistance. The input resistance is roughly equal to the smallest base bias resistors, $R_{\text{in}} = 2\,\text{k}\Omega$. Then

$$G_{vo} = A_{vo}\frac{R_{\text{in}}}{R_{\text{sig}} + R_{\text{in}}} = -7 \times \frac{2}{1+2} = -4.7$$

3. Biasing. Derive the expressions for I_C and for I_E for this circuit. What makes this a better circuit for obtaining a particular value of I_C than the circuit in question 1?



We see that the current through R_C is I_E and can wirte

$$V_{CC} = I_E R_C + \frac{I_E}{\beta + 1} R_B + V_{BE}$$

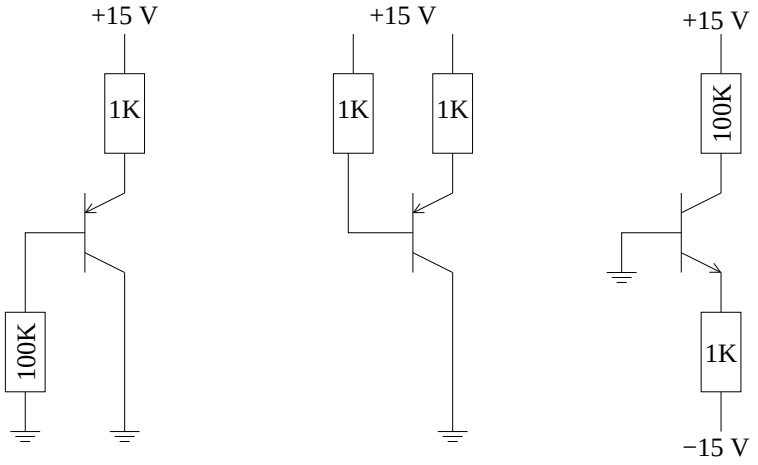
$$I_E = \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{\beta+1}}$$

and

$$I_C = \alpha I_E = \alpha \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{\beta+1}}$$

The circuit is better at biasing I_C and I_E, because there is a weaker dependence on both V_{BE} and β than the circuit in question 1. The circuit in question 1 has a linear dependence on β.

4. DC analysis. For these circuits give the three terminal voltages and the three terminal currents, and state the operating mode. Assume $\beta = 100$ for all.



For the first circuit it is is active mode because the bias cannot be at a lower voltage than the collector. We have $V_C = 0\,\mathrm{V}$, and

$$I_B R_B + V_{EB} + (\beta + 1)\, I_B R_E = V_{EE}$$

$$I_B = \frac{V_{EE} - V_{EB}}{R_B + (\beta + 1)\, R_E} = \frac{15 - 0.7}{100 + 101} = 71\,\mu\mathrm{A}$$

$$I_E = (\beta + 1)\, I_B = 101 \times 0.071 = 7.2\,\mathrm{mA}$$

$$I_C = \beta I_B = 7.1\,\mathrm{mA}$$

$$V_B = I_B R_B = 100 \times 0.071 = 7.1\,\mathrm{V}$$

$$V_E = V_B + V_{EB} = 7.1 + 0.7 = 7.8\,\mathrm{V}$$

For the second circuit we can see that it is in cutoff mode. No current is flowing through the transistor and thus $I_B = I_C = I_E = 0$ and $V_B = V_E = V_{EE} = 15\,\mathrm{V}$. $V_C = 0\,\mathrm{V}$.
For the third circuit we have $V_B = 0\,\mathrm{V}$ and $V_E = -0.7\,\mathrm{V}$, and thus

$$I_E = \frac{V_E - V_{EE}}{R_E} = \frac{-0.7 + 15}{1} = 14.3\,\mathrm{mA}$$

it looks like the circuit is in saturation mode because of the very large ratio of R_C and R_E. In that case $V_C = V_E + V_{CEsat} = -0.7 + 0.2 = -0.5\,\mathrm{V}$, and then

$$I_C = \frac{V_{CC} - V_C}{R_C} = \frac{15 + 0.5}{100} = 0.16\,\mathrm{mA}$$

The large difference between I_C and I_E confirms saturation mode.