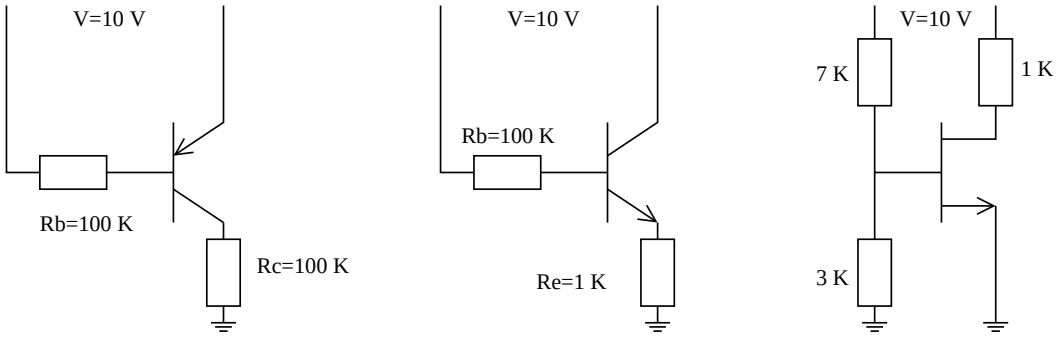
# EE 321 Analog Electronics, Fall 2011
# Exam 3 November 30, 2011
# Solution

**Rules: This is a closed-book exam. You may use only your brain, a calculator and pen/paper. Each numbered question counts equally toward your grade.**

**Note: The questions are designed to test your conceptual understanding, not your ability to do many pages of math. If you find yourself doing long calculations there is a high probability that you are doing something wrong.**

## DC analysis

1. **Find all the voltages and currents in this circuit. Assume $\beta = 100$, $V_t = 1\,\mathrm{V}$, and $k_n' \frac{W}{L} = 1\,\mathrm{mA/V^2}$.**




For the first circuit we see that it is in cutoff mode, so no current is flowing, thus $I_B = I_C = I_E = 0$, and then the voltages are $V_B = V_C = V = 10\,\mathrm{V}$, and $V_E = 0\,\mathrm{V}$.

For the second circuit it is on, and must be in active mode. We can write

$$V = I_B R_B + V_{BE} + (\beta + 1)\, I_B R_E$$

or

$$I_B = \frac{V - V_{BE}}{R_B + (\beta + 1)\, R_E} = \frac{10 - 0.7}{100 + 101} = 46.3\,\mu\mathrm{A}$$

Then

$$I_C = \beta I_B = 100 \times 46.3 = 4.63\,\mathrm{mA}$$

and

$$I_E = (\beta + 1)\, I_B = 101 \times 49.8 = 4.67\,\mathrm{mA}$$

The voltages are

$$V_B = V - I_B R_B = 10 - 49.8 \times 10^{-6} \times 100 \times 10^5 = 5.37\,\mathrm{V}$$

$$V_C = V = 10\,\mathrm{V}$$

$$V_E = I_E R_E = 4.67 \times 1 = 4.67\,\mathrm{V}$$

The third circuit is a NMOS. We have immediately $V_{GS} = 3\,\mathrm{V}$ as a voltage division of $10\,\mathrm{V}$, and $V_S = 0\,\mathrm{V}$. Also $I_G = 0$ of course. Let's assume saturation mode. In that case we have

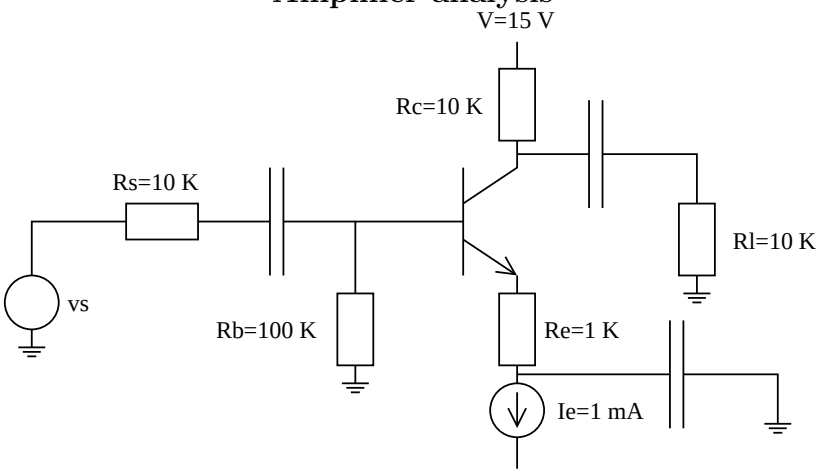
$$I_D = \frac{k'_n}{2}\frac{W}{L}\left(V_{GS} - V_t\right)^2 = \frac{1}{2}\left(3-1\right)^2 = 2\,\mathrm{mA}$$

and

$$V_D = V - I_D R_D = 10 - 2 = 8\,\mathrm{V}$$

which is consistent with the saturation mode assumption.

**Amplifier analysis**




assume $\beta = 100$

2. **Explain why this circuit has $A_{vo} \approx -10$ and $V_C \approx 5\,\mathrm{V}$ (you may assume these values in the following questions).**

   The gain is approximately the collector resistance divided by the emitter resistance. Ignoring $r_e$ we get a gain of 10. The bias current is $1\,\mathrm{mA}$, and $V_C = V_{CC} - I_C R_C = 10 - 1 \times 10 = 5\,\mathrm{V}$.

3. **What is the smallest signal output permitted while the BJT remains in the active mode? (careful, the base is not at ground)**

The edge of active mode corresponds to $V_{CB} = -0.4\,\mathrm{V}$. The base voltage is $V_B = -I_B R_B = \frac{I_E}{\beta+1} R_B = -\frac{1}{101} \times 100 = -0.99\,\mathrm{V}$. Thus the smallest allowed $v_C = -0.99 - 0.4 = -1.34$, and the smallest signal, $v_c = -1.34 - 5 = -6.34\,\mathrm{V}$.

**4. Draw the small-signal model for the circuit.**

**5. What is $R_{\mathrm{in}}$, and what is $G_v$?**

$R_{\mathrm{in}}$ is the parallel combination of $R_B$ and $(\beta+1)\,r_e + R_E$. First get

$$r_e = \frac{V_T}{I} = \frac{25}{1} = 25\,\Omega$$

next,

$$R_{\mathrm{in}} = R_B || \,(\beta+1)\,(r_e + R_E) = 100||101 \times 1025 = 50.9\,\mathrm{k}\Omega$$

Next, $G_v$ is $A_{vo}$ with a voltage division on the output and a voltage division on the input

$$G_v = \frac{R_{\mathrm{in}}}{R_S + R_{\mathrm{in}}} A_{vo} \frac{R_C}{R_L + R_C} = -\frac{50.9}{10 + 50.9} \times 10 \times \frac{10}{10 + 10} = -4.18$$