EE 322 Advanced Analog Electronics, Spring 2008
Test 3 solutions
April 18, 2008, 10:00-10:50

Each numbered question in this test counts equally toward the test grade. All of the questions in this test are conceptual, and none of them require long derivations.

Phase-locked loop

1. **A PLL consists of an XOR (Type I) phase detector, which outputs $0 - V_{CC}$ as the phase varies $0 - 2\pi$, a LP filter, and a VCO for which the frequency varies linearly from $20\,\text{kHz}$ to $150\,\text{kHz}$ as the voltage varies from 0 to V_{CC}. If the input signal is $30\,\text{kHz}$, what is the phase difference between input and output signal?**

   The relationship between phase difference and output voltage of the phase detector is

   $$V_o = \Delta\phi_i \frac{V_{CC}}{2\pi}$$

   The relationship between input voltage of the VCO and output frequency is

   $$f = 20\,\text{kHz} + \frac{V_i}{V_{CC}} 130\,\text{kHz}$$

   The input of the VCO must equal the output of the phase detector, so we have

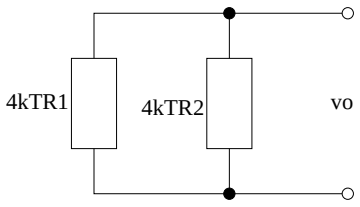
   $$\Delta\phi_i \frac{V_{CC}}{2\pi} = (f - 20)\,\frac{V_{CC}}{130}$$

   Inserting $f = 30$ we get

   $$\Delta\phi_i = \frac{2\pi(30 - 20)}{130} = 0.48$$

Noise

2. **What is the noise power spectrum of two resistors R_1 and R_2 in parallel? You may want to use superposition and think of the circuit as a voltage divider.**



   The noise from R_1 appears on the output divided accordig to $\frac{R_2}{R_1+R_2}$, because the relative to the R_1 noise source, v_o is measured across R_2 only, and the noise sources is across both resistors. Similar for R_2 noise, so we can write

$$v_o = v_1 \frac{R_2}{R_1 + R_2} + v_2 \frac{R_1}{R_1 + R_2}$$

For the noise power we then get (squaring)

$$\begin{aligned} e_o^2 =& e_1^2 \left(\frac{R_2}{R_1 + R_2} \right)^2 + e_2^2 \left(\frac{R_1}{R_1 + R_2} \right)^2 \\ =& 4kT \frac{R_1 R_2^2 + R_2 R_1^2}{(R_1 + R_2)^2} \end{aligned}$$

3. **An amplifier is a cascade of three amplifier stages, the first has input noise e_{na1} and gain K_1, the second has input noise e_{na2} and gain K_2, and the third has input noise e_{na3} and gain K_3. If these are the only noise sources, what is the noise power spectrum at the output of the third amplifier? In which stage should you be most careful about minimizing noise, and why?**

   At the output of amplifier stage 1, the noise is

$$e_{o1}^2 = K_1^2 e_{na1}^2$$

   At the output of amplifier stage 2, the noise is

$$e_{o2}^2 = K_2^2 \left(K_1^2 e_{na1}^2 + e_{na2}^2 \right)$$

   At the output of amplifier stage 3, the noise is

$$\begin{aligned} e_{o3}^2 =& K_3^2 \left[K_2^2 \left(K_1^2 e_{na1}^2 + e_{na2}^2 \right) + e_{na3}^2 \right] \\ =& K_3^2 K_2^2 K_1^2 e_{na1}^2 + K_3^2 K_2^2 e_{na2}^2 + K_3^2 e_{na3}^2 \end{aligned}$$

   The noise on the first amplifier is amplified the most, and dominates the output, so that is where we have to focus attention on noise reduction (Assuming that K_1, K_2, and K_3 are all larger than 1).

Current Feedback Op-amp

4. **How is bandwidth defined? Explain in words and/or with math why we usually say that the bandwidth of a CFOA is independent of closed-loop gain. And why is bandwidth not independent of gain for the VFOA?**

   Bandwidth is defined as the point where the error (the difference between positive and negative inputs) is comparable to the input signal. It occurs at the point where the closed loop gain approaches the open-loop gain, $\frac{1}{\beta} = A$, or $A\beta = 1$.

For the current feedback op-amp the feedback β is equal to the negative of the coefficient which converts from output voltage, V_{out}, to current in the CFOA (it is the negative because that definition straddles the inverting input). Let's assume a non-inverting, and set the positive input to zero. Let's set the positive input and the source input (assuming an inverting configuration) to zero, then the current node equation at the invering input is

$$I + \frac{V_{\text{out}} - V_-}{Z_F} + \frac{-V_-}{Z_G} = 0$$

Now, $V_- = -IZ_B$, so we insert

$$I + \frac{V_{\text{out}} + IZ_B}{Z_F} + \frac{IZ_B}{Z_G} = 0$$

$$I + \frac{V_{\text{out}}}{Z_F} + I\frac{Z_B}{Z_F} + I\frac{Z_B}{Z_G} = 0$$

Now if we assume that $Z_B \ll Z_F$ and $Z_B \ll Z_G$, then the three I terms reduce to just I, and we get

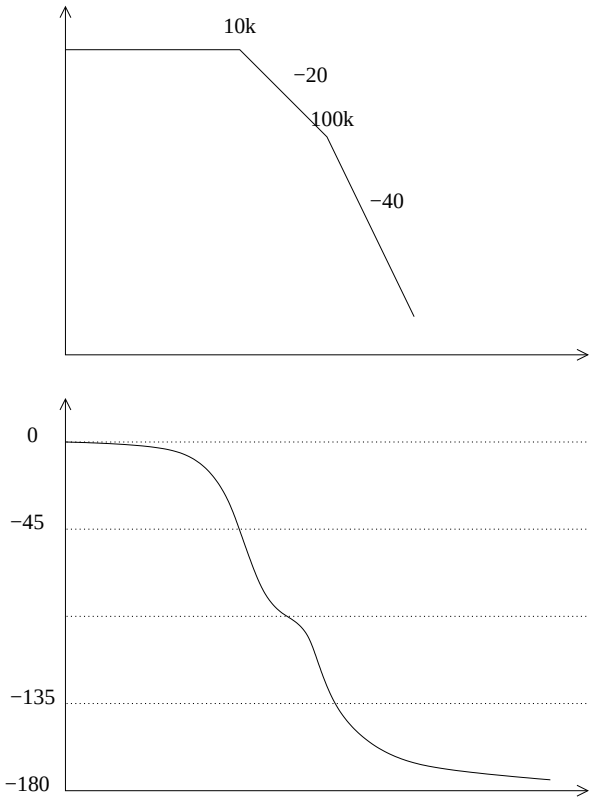
$$\beta = -\frac{I}{V_{\text{out}}} = \frac{1}{Z_F}$$

We see that β is independent of the closed-loop gain, depends only on Z_F. Therefore, the frequency at which the β reaches one is also independent of closed-loop gain.

If we perform the same calculation for the VFOA, we find that β is unitless, and contains the ratio of Z_F/Z_G. Thus, for the VFOA, β does depend on the closed-loop gain, and thus the frequency at which $\beta = 1$ does depend on closed-loop gain.

Stability

5. **An op-amp (VFOA) has a pole at $10\,\text{kHz}$, and another pole at $100\,\text{kHz}$. Its DC gain is 10^6. Draw the open-loop transfer function (amplitude and phase).**



6. **What is the closed loop gain corresponding to $45°$ phase margin? What happens if you make the closed loop gain smaller? larger? Design a inverting amplifier which has this phase margin.**

   $45°$ phase margin happens at the knee of the 100 kHz pole. We want the loop gain, $|A\beta| = 1$ at that point. At that point, $A = 10^5$, so that $\beta = 10^{-5}$. The closed-loop gain is $K = \frac{1}{\beta} = 10^5$.

   If we make the closed-loop gain larger, we make β smaller thus making the loop gain smaller. This means we reach unity magnitude loop gain at lower frequency. So we increase the phase margin if we make the closed-loop gain larger.

   If we make the closed-loop gain smaller, we make β larger thus maiking the loop gain larger. This means we reach unity magnitude loop gain at higher frequency. So we decrease the phase margin if we make the closed-loop gain smaller.

   An inverting amplifier with this closed-loop gain must have resistor ratios of 10^5, so we could choose $R_F = 10\,\mathrm{M}\Omega$, and $R_G = 100\,\Omega$.

7. **Using magic you add another pole at $1\,\mathrm{MHz}$. What closed-loop gain should you choose to cause oscillations? At what frequency will the circuit oscillate? Approximate values estimated from a graph are acceptable.**

   If we add a third pole, the phase will reach $-180°$ between the second and third pole. So it is in this region that we want the loop gain to be unity. At the second pole the open-loop gain is 10^5. At the third pole the open-loop gain is 10^3. Halfway between the two the open-loop gain is 10^4. So if we choose $\beta = 10^{-4}$ we get a loop-gain of -1. So

the closed-loop gain should be $\frac{1}{\beta} = 10^{-4}$. The frequency where that happens is halfway between $100\,\mathrm{k\Omega}$ and $1\,\mathrm{M\Omega}$ on a log scale, roughly $300\,\mathrm{kHz}$.