EE 322 Analog Electronics, Spring 2010
Exam 3 May 7, 2010

Amplifier Stability and stability

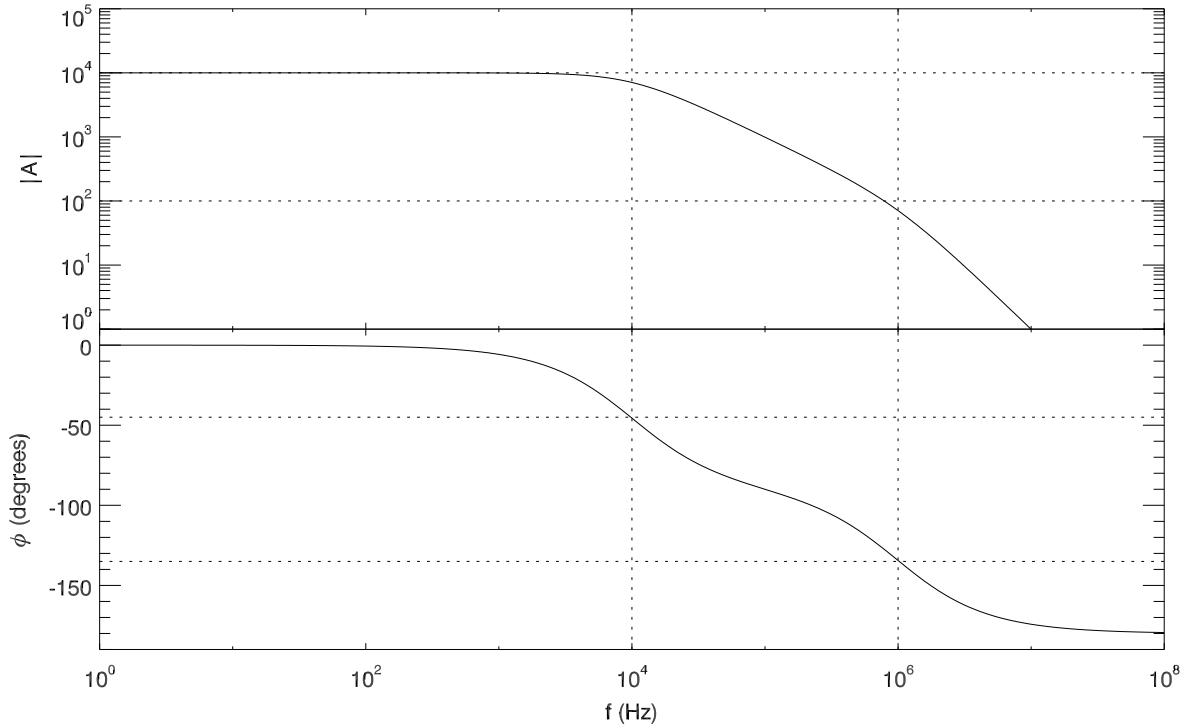
A differential amplifier has a transfer function, A, with DC open-loop gain of 10^4, and poles at 10^4 Hz, and 10^6 Hz. You may assume that the poles are widely spaced such that as the frequency of a pole is passed, the full phase shift is realized before the next pole is encountered.

1. **Plot and label amplitude and phase of A as a function of frequency, up to the unity gain frequency. What is the unity gain frequency?**

   The transfer function is

   $$A = \frac{10^5}{\left(1 + j\frac{10^4}{2\pi f}\right)\left(1 + j\frac{10^6}{2\pi f}\right)}$$

   The amplitude and phase of that function are here

   Unity gain occurs at a frequency of 10^7 Hz.

2. **What negative feedback factor, β, will result in a gain margin of 45°? What is the corresponding closed-loop gain of a non-inverting amplifier? Is this a minimum or maximum closed-loop gain to achive at least that phase margin?**

   A phase margin of 45° is a phase of $-135°$, which corresponds to $A = 10^2$, so we need a feedback factor of $\beta = 10^{-2}$. The corresponding closed loop gain is $G = 1 + \frac{1}{\beta} \approx \frac{1}{\beta} = 10^2$. This is the minimum gain that will satisfy the phase margin.

3. **The differential amplifier has a output resistance of 10 kΩ, and we wish to dominant-pole-compensate it to a phase margin of 45° at unity-open loop gain. Draw the circuit as a non-inverting amplifier and choose the value of the capacitor.**

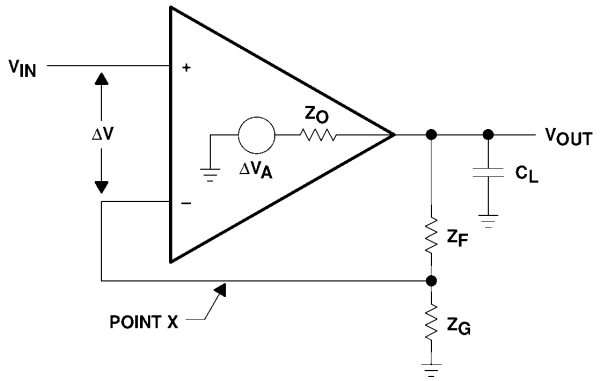
We want the modified function to have unity gain at the frequency of the first pole in the original open-loop gain, so we should add a pole with a frequency of 1 Hz, because it will drop the open-loop gain by 10^4 at the pole at 10^4 Hz. Combining the capacitor with the output resistance of the op-amp we get

$$1\,\text{Hz} = \frac{1}{2\pi R_o C}$$

or

$$C = \frac{1}{2\pi R} = \frac{1}{2\pi \times 10^4} = 16\,\mu\text{F}$$

Here is the circuit



Two-stage amplifier

A NPN BJT differential pair is biased with a 1 mA constant current source. Assume active mode operation. We take a single-ended output. Assume $\beta = 100$.

4. **What is the transconductance of the BJTs? What value of collector resistances will produce a gain (between the differential input and the single-ended output) of 100?**

The transconductance of BJT is

$$g_m = \frac{i_c}{v_{be}} = \frac{I_C}{V_T}$$

In this case we have $I_C = \alpha\frac{I}{2}$, $I = 1\,\text{mA}$

$$g_m = \frac{100}{101}\frac{\frac{1}{2}}{25} = 0.02\,\Omega^{-1}$$

The relationship between output voltage and input voltage is

$$v_o = \frac{v_{id}}{2} g_m R_C$$

so we get

$$R_C = \frac{2}{g_m}\frac{v_o}{v_{id}} = \frac{2}{0.02} \times 100 = 10\,\mathrm{k\Omega}$$

5. Show that the common-mode gain is $-\frac{\alpha R_C}{2R_{EE}}$ (to a good approximation). If the current source has a output resistance of $R_{EE} = 1\,\mathrm{M\Omega}$, what is the CMRR? What would be the CMRR if we took a differential output instead?

As we increase the common-mode voltage on the base, and assume that v_{BE} is constant, we increase the emitter voltage by that same amount, and thus the current through the resistor by

$$i_{ec} = \frac{1}{2}\frac{v_{ic}}{R_{EE}}$$

(it is half because the current is shared between two BJTs). The voltage on the output is (ignoring signs)

$$v_{oc} = i_{cc} R_C = \alpha i_{ec} R_C = \alpha \frac{1}{2}\frac{v_{ic}}{R_{EE}} R_C = \frac{\alpha R_C v_{ic}}{2R_{EE}}$$

Re-arranging it to the get common-mode gain we get

$$A_C = \frac{v_{oc}}{v_{ic}} = \frac{\alpha R_C}{2R_{EE}}$$

which evaluates to

$$A_C = \frac{\frac{100}{101} \times 10^4}{2 \times 10^6} = 4.96 \times 10^{-3}$$

The common-mode rejection ratio is then

$$\mathrm{CMRR} = \frac{A_d}{A_C} = \frac{100}{4.96 \times 10^{-3}} = 2.02 \times 10^4$$

6. The output is connected to the base of a common-emitter amplifier, biased to give a DC emitter current of 1 mA. How does the gain in question 4 change with this addition? How might one mitigate some of this gain change?

The input resistance of the base is connected in parallel with the collector resistance, R_C. The base input resistance is

$$r_\pi = \frac{\beta V_T}{I} = 100 \times \frac{25}{1} = 2500\,\Omega$$

Placing that in paralle with $R_C = 10\,\mathrm{k}\Omega$ we get

$$r_\pi || R_C = 2500 || 10^4 = 2000\,\Omega$$

Attaching the common-emitter transistor thus reduces the the gain by a factor of 5 to 20. We can mitigate this gain drop by increasing the input resistance on the base by connecting a large resistors (for example $100\,\mathrm{k}\Omega$) in series with the base. However this may also require changing the biase DC voltage of the common-emitter.