Lab 12 and 13
Discrete Component Operational Amplifier

In this lab we will build and test a simple BJT operational amplifier from discrete components. The circuit that we will use is presented and discussed by Sedra and Smith in Example 7.4 (pages 758-760) and in Section 7.7 and Example 7.5 (pages 760-766) (we will make many changes in the circuit as indicated below). It utilizes differential transistor pairs to amplify the difference between the (+) and (-) inputs, and current mirrors (rather than resistors) to bias the transistors. Successive stages of the amplifier are direct coupled to eliminate bypass or coupling capacitors and to allow DC operation. For comparison, the circuitry of a 741 amplifier is given on p. 894 of Sedra and Smith.

NOTE: It will be important to lay out the amplifier neatly on your breadboard. It will probably take you two lab periods to finish. Use bus lines for the $\pm 15\,\mathrm{V}$ supplies, and lay the circuit out between two sets of bus lines from the bottom to top of the breadboard. (This puts the input stage furthest from the supply and decreases the chances that feedback through the supply bus will cause the circuit to oscillate.) The circuitry is more complicated than you may be used to breadboarding, and MOST PROBLEMS WILL COME FROM WIRING MISTAKES. Take the time to wire your circuit CAREFULLY and NEATLY to avoid mistakes.

Pre-lab

1. Obtain data sheet for the CA3086 and possibly the 2N390X transistors as necessary.
2. Draw the circuit you are building (it is different from the circuit in Sedra and Smith).
3. Specify the values of all resistors.

Part A: Bias Voltages and DC currents

Construct and test the amplifier in stages as described below. Use then 2N3906 PNP and 2N3904 NPN transistors for Q_7, Q_8 and the current mirrors. Use the transistor array CA3086 for the differential pairs Q_1, Q_2, Q_4 and Q_5. Handel this chip with care. As the construction proceeds you will probably have to adjust some component values slightly to get the proper bias. Note the bias voltages and currents directly on your schematic, as in Figure 7.44.

1. Use $\pm 10\,\mathrm{V}$ supplies. The maximum collector to substrate voltage for the CA3086 is $20\,\mathrm{V}$. This will reduce all the bias voltages. Keep the currents the same as in figure 7.44, but reduce the voltages to 66% by reducing the resistors to 66% of the values in the figure.
2. Construct the first mirror, Q_9 and Q_3. Test this current mirror with a load of about $10\,\mathrm{k}\Omega$.

3. Construct the first stage differential amplifier (Q_1-Q_2) using the CA3086. According to the data sheet the substrate (pin 13) must be connected to the most negative point in the circuit (find this in the data sheet and follow their suggestion about a capacitor). Include a 1 kΩ pot in series with one collector resistor and 500 Ω in series with the other. (This will be used to fine tune the bias voltages after the entire amplifier is built.)

4. With both inputs grounded, measure the bias voltages at each point in the circuit, starting with Q_9, then Q_3, etc. Remember that each transistor should be in its active mode (0.6-0.7 V base-emitter voltage and base-collector reverse-biased (or zero)). Check this for each transistor as you go, and note the values on your schematic. Measuring bias voltages is the BEST WAY to troubleshoot a circuit, and if you ever have problems with the circuit not working, you can usually find the problem by rechecking the bias values.

5. Note that the bias voltages on the two collectors can be used to compute the collector currents. Do this and compare with their design values. (The currents can be equalized by adjusting the 1 kΩ potentiometer.) The total bias current can also be determined by measuring the voltage across R_E of the current mirror. Do this.

6. Test the operation of the first stage by applying a sine wave from your signal generator to one of the inputs. (Leave the other input grounded.) By displaying one of the collector voltages vs. the input voltage in x-y mode on your scope, you should be able to reproduce the curves of Figure 7.6 in your text. Carefully plot both collector waveforms on the same plot. You should be able to estimate the small-signal gain of the first stage by measuring the slope at zero input. Compare with the theoretical gain $\frac{g_m R_C}{2}$.

7. Add the second stage biasing current mirror. In the design the collector current of Q_6 is 4 times that of Q_3, a transistor of 4× the junction area would need to be used. This could be done by connecting 4 transistors in parallel, as in Figure 7.44. Use only one transistor. The current in the Widlar current mirror for this stage can be increased by changing the emitter resistor. Note that R_E will have to be smaller than before. Calculate the value by assuming the V_{BE} won't change much. It is very important to get this current close to 2 mA. Test it with a 2 kΩ load.

8. Add the second stage differential amplifier using two more transistors in the CA3086.

9. Connect the two stages and measure the bias levels in the same manner as before (amplifier inputs grounded). Compare with the expected bias voltages and currents. Note that the collector voltage of Q_5 will provide the bias for the remaining stages and must be close to +8 V. If it is not check the bias current and make sure both inputs are the same. It is not necessary to test this stage with a sinusoidal input; if the bias levels are correct the circuit will function properly.

10. Add the PNP level converter (Q_7) and emitter-follower output driver (Q_8). The goal here is to achieve 0 V DC bias at the output of the amplifier; if the previous stage bias is close enough you should be able accomplish this using the 1 kΩ potentiometer (carefully consider where to put it). NOTE that the output transistor will be dissipating some power (how much?). The 2N3904 should be able to handle it, as it has a 1.5 W rating at 25° C. The potentiometer in the first stage serves as a DC offset adjust. Is the adjustment fine or coarse?

Part A: Bias Voltages and DC currents

11. Bypass the power supply lines near the amplifier with 0.1 or 0.01 μF capacitors. Measure the open-loop gain of the op amp at 1 kHz. In Example 6.3, the gain is computed stage by stage to be a total of about 8500 (p. 765). Apply a suitably small signal (1 mV p-p or less) to the (+) or (-) input to measure the gain, leaving the other input grounded. Use a voltage divider of low source resistance (50 ohms) to produce the input signal. (A larger source resistance would alter the bias voltages in the circuit.) With the large gain and small input signals you will have to take care about how everything is grounded. The output voltage should swing both positive and negative. Measure the overall gain, and compare with theory. (As an option, measure the gain at each stage.)

12. Briefly measure the $3\,text{-}dB$ frequency of the amplifier. To do this, you may have to reduce the input signal amplitude if the output amplitude is limited by the slew rate as the signal frequency is increased. (Option: What is the measured slew rate?) Can you measure the unity gain frequency?

13. As it stands, the Op-Amp is not compensated and would probably oscillate if you tried to apply feedback (why?). Compensate the op amp by placing a 0.01 μF capacitor between the collectors of Q_1 and Q_2. Measure the new break point and unity gain frequency. Make a sketch to scale of the asymptotic Bode plot for the uncompensated and compensated open loop gain.

14. Use the compensated Op-Amp to implement an inverting gain of 10 amplifier. Measure the bandwidth of the amplifier and check if this is what you would expect from the open loop gain. The frequency response may be peaked just below the 3 dB frequency; this means that there is a pole pair close to the imaginary axis at this frequency and therefore that the step response will have overshoot. Test and document this with a square wave input. The ringing can be eliminated by increasing the compensation capacitor to 0.1 μF. Document the effect on the step response and closed loop bandwidth.

15. (Optional) If you have gotten this far and want to do more (and earn extra credit), try measuring various non-ideal things about the Op-Amp, such as its slew rate, saturation values, input noise, input DC offset, input bias current, common-mode rejection, etc.