Preliminary design

We will perform a preliminary analysis of each of the subsystems. This table lists people/subsystem associations. Some sub-systems (such as the CMS) are more complex.

Name	CPU	SPA	VVS	CMS	Power	FS
Huynh					X	X
Landavazo			X			X
Marohn	X	X				
Mason	X	X			X	
Quiroga				X		
Ravindran				X	X	
Yelton			X	X		
Wootton		X				

1 Subsystem brief descriptions and specs

1.1 CPU

The CPU is the brain of the experiment. It communicates with the spacecraft through the SPA interface (a part of which might even be implemented on the CPU as an I^2C interface). This communication consists of responding to commands and transmitting data. It also commands the VVS to change voltage levels (perhaps through a DAC built into the CPU). It collects data from the CMS (possibly through a ADC built into the CPU). It also stores data collected and perhaps performs some simple computations.

1.2 SPA

The SPA implements the SPA-1 interface to the rest of the satellite. It consists of 4 pins, one of which is ground, another 5 V power supply, and two are communications pins implementing I^2C.

1.3 VVS

The VVS (Variable Voltage Supply) biases the probe with a voltage according to the programmed sweep from the CPU. It receives commands from the CPU to set the voltage level. It can bias at both negative and positive voltages. The VVS may also need to provide specific known inputs directly to the CMS for calibration purposes, as commanded by the CPU.

1.4 CMS

The CMS (Current Measurements System) measures the amount of current flowing through the probe. It is able to measure both positive and negative currents, and should be able to measure currents over a very wide range and provide reasonable resolution across that range. We are initially considering 6 orders of magnitude.

1.5 Power

The power sub-system takes as input the 5 V input from the SPA and provides on the output all the voltages needed by the instrument. One guess at what voltages may be needed is 3.3 V and ± 15 V.

1.6 FS

The FS (Fake Satellite) is used during testing to emulate the satellite side of the interface with the satellite. It should be able to provide and accept all the signals expected by the instrument.

2 Preliminary design considerations and questions

In the following are a list of specific and non-specific questions relating to the choice of implementation for the different sub-systems. In some cases the specifications are not complete, and the specs that we choose will depend on what we can realistically expect. We want a discussion and evaluation of what to expect, and some preliminary recommendations of approaches and components to use.

2.1 CPU

We want to analyze the CPU used in the Taylor U. System. Is it compatible with the SPA interface? Are there good programming tools available? Is there on board flash that can be easily permanently programmed? Are there useful evaluation boards available that can be used for code development before the flight board is ready? How much RAM is available? How much flash? What I/Os and ADC and DAC are available?

2.2 SPA

Read the SPA document in enough detail to understand the protocol and have some idea of how it might be implemented on the CPU. This requires some communication with whoever is analyzing the CPU. The SPA interface may also place constraints on our power supply. Is there any specific hardware that is needed (other than the connector) to use the SPA interface? Does the spacecraft document specify what connector to use?

2.3 VVS

Are there any useful implementations of the VVS other than a DAC followed by a op-amp? What components did Taylor U use? What can those do? Are there alternatives? Are there power consumption issues? How many voltage levels do we want? Absolute minimum is probably 16 and 256 is probably more reasonable. That is the number of voltage levels between the most negative and the most positive voltage. Let's assume for now that the output range is $-10\,\mathrm{V}$ to $+10\,\mathrm{V}$. How fast is the DAC? If we want to cycle through all 256 levels in 0.01s, 0.1 s, 1 s, 10 s, does that pose any problems? The speed of the VVS will probably also depend on how much downlink bandwidth we are assigned for data. The downlink number is still TBD.

2.4 CMS

There CMS is probably the most complicated system. It needs to measure currents over many orders of magnitude. For now we assume 6 orders of magnitude, but we will get some more accurate numbers from Dr. Dale Ferguson at AFRL Albuquerque. He will be running a model for us over the next few days. For the time being let's assume a typical current of $1\,\mu\mathrm{A}$, with variation of plus or minus three orders of magnitude. That means $1\,\mathrm{nA}$ to $1\,\mathrm{mA}$. If that turns out to be unreasonable, what range might be reasonable?

There are several possibilities which we can look into as far as the CMS is concerned.

There is (1) The Taylor university concept of a logarithmic amplifier, (2) the idea of multiple parallel amplifiers of different gains, and (3) an integrator with trigger, where the time from reset to trigger is inversely proportional to the current.

Which of these three systems make most sense from the standpoint of ease of implementation and ease of calibration?

2.4.1 CMS - Taylor U We need to analyze the Taylor U log amplifier and understand it in detail. The two transistors create effectively a resistor which has approximately an exponential relationship between voltage and current, resulting in a output which is approximately the log of the input, with the sign related to the sign of the current. How much gain does the second stage amplifier provide? How can we (or Taylor U) be confident of a specific relationship between current and output voltage given that I_S and V_T can vary some on the transistors? In other words, how can they be confident of the IV characteristic of the transistors, or is the system designed such that this does not matter? Are these precision transistor for which I_S and V_T are known?

2.4.2 CMS - parallel An alternative solution is to use a number of parallel linear amplifiers with different gains covering the entire range. In that case, how many amplifiers will we need? The answer actually depends on how many bits of precision we want. Perhaps a good estimate is 4-6 amplifiers for the 6 orders of magnitude. In order to use this scheme we need a pre-amplifier which converts the current into a voltage which is then distributed among the parallel amplifiers. In order for the amplifier to not saturate for any current the output voltage will need to be quite small. In that case, is there an issue with the offset voltage? Are there op-amps with extremely small offset voltages that might be capable of dealing with this? Remember the offset voltages are amplified by the gain of the amplifier. Notice that for calibration the Taylor U has the facility to inject specific known currents into the log amplifier, likely selected with output pins on the CPU.

2.4.3 CMS - integrator Another possibility is to use an integrator. The current is fed directly into an integrator, and when the voltage reaches a particular level it triggers a CPU timer to stop and the integration time can be read out. The difficulty is that the trigger level can be negative so we need a circuit that can deal with both a positive and a negative trigger voltage. And we need some way of resetting the circuit after the trigger, discharging the capacitor by shorting it. In order for this to work we also need amplifiers with small bias currents, and we need a way to inject zero current into the input (selected with a CPU output pin) in order to measure the bias current. A problem with this system is that the integration time varies with the the current, and if the current varies by 6 orders of magnitude so does the integration time. Being able to switch capacitors on the integrator would help, but would add complication to the instrument. Is this system at all feasible?

2.5 Power

We are provided a single 5 V power line from the SPA interface. We need to generate voltages for the CPU, VVS, and the CMS. My first guess is that we will need a small voltage, 3 or 3.3 V, and two large voltages, ± 15 V. The Taylor U instrument uses a switching power supply (DC-DC converter) and that is almost certainly the correct approach. We want to get some suggestions for DC-DC converters. They need to supply enough power for our instruments, but not much more than that. That number is still TBD, but a good guess could be a few mA to a few 10's of mA. The Taylor U switching regulator requires a lot of external circuitry.

Is there a component available which requires less external circuitry, and is still compact?

2.6 FS

We want this system to consist of a desktop computer (or laptop), which is connected to a microcontroller which implements the SPA-1 interface communications with the satellite. The interface on the computer and the programming of the microcontroller should be flexible so that we can perform a variety of tests. Some interactive tests are useful as are long-term unattended tests.