Homework Assignment 3
Circuit schematics in multisim
Due February 7, 2011

This is a group homework. The homework assignment is to create a multisim schematic for your subsystem. The schematic should include all the components needed for your subsystem as well as names of nodes that will connect to other subsystems. Also label headers that you think will be needed as test points. The groups are:

Subsystem	Group members
CPU	Marohn, Mason
SPA	Mason, Marohn
VVS	Yelton, Landavazo
CMS	Guilette, Ravindran, Quiroga, Yelton
Power	Ravindran, Huynh, Mason

The person listed first is the coordinator for that subsystem for this homework assignment. I want to receive the response from that person. Bring the response to class on Monday electronically, or e-mail it to me before class. Please coordinate among yourselves to complete the assignment. You can find everyone's e-mails at `http://www.ee.nmt.edu/~anders/courses/ee491s11/team/contactList.html`. If different team members contributed very differently to the answer, please indicate what percentage each contributed.

In some cases some components, such as surface mount resistors, capacitors, and inductors, and such are not yet specified by part number. In those cases it is OK to use generics, with the intent that we will determine the part numbers for board layout and manufacturing shortly at the next stage.

Detailed instructions for each subsystem

- **CPU:** In addition to the schematic also create a brief outline of software in pseudocode, indicating where there are still some unknowns.

- **VVS:** Use the DAC on the CPU and design the amplifier needed to go from the 0-3 V DAC output to -20 to +20 V. The best way to do that may be through an inverting summer where one of the inputs is the -20 V supply. So +3 V on the DAC should correspond to -20 V on the output and 0 V on the DAC should correspond to +20 V on the output. When selecting resistors make sure that the DAC output is capable of sourcing and sinking the necessary current. Use large, but not extremely large, resistors, to minimize current and power consumption. Make the resistors large enough that they do not dominate power. You may need to ask the CPU team how much current the DAC can source and sink.

- **Power:** In the schematic include headers that allow us to inject the voltages -20 V, +20 V, and 3.3 V (for the CPU) directly with bench supplies during testing. This way we will be able to bypass the power supply chips during the early testing stages. This is useful because the chips are very difficult to work with because of their small

size. Think of a test setup for testing the circuit diagram surrounding the switching regulator chips.

- **SPA:** There is relatively little to do hardware-wise for this one as it consists just of a connector which we don't yet know what is. This multisim schematic could therefore be drawn as four header pins for now, each leading to a named node. As far as software, do a preliminary definition of what should be our responses to different commands from the spacecraft.

- **FS:** On Friday February 4 I will be meeting with Craig Kief from COSMIAC in Albuquerque to discuss whether we can use their equipment as a FS. Therefore no activity on this subsystem until I report back.

- **CMS:** The MAX4206 will not work for this subsystem because it does not accept the large voltage bias on the input. Therefore please follow the design of the Taylor University system. I have the MAT14 chips available for this. I found that multisim has spice models for MAT04 chips (pick the SOIC version). Please check into whether you can use those, whether they have same response and same pin-out as the MAT14. I think they do.