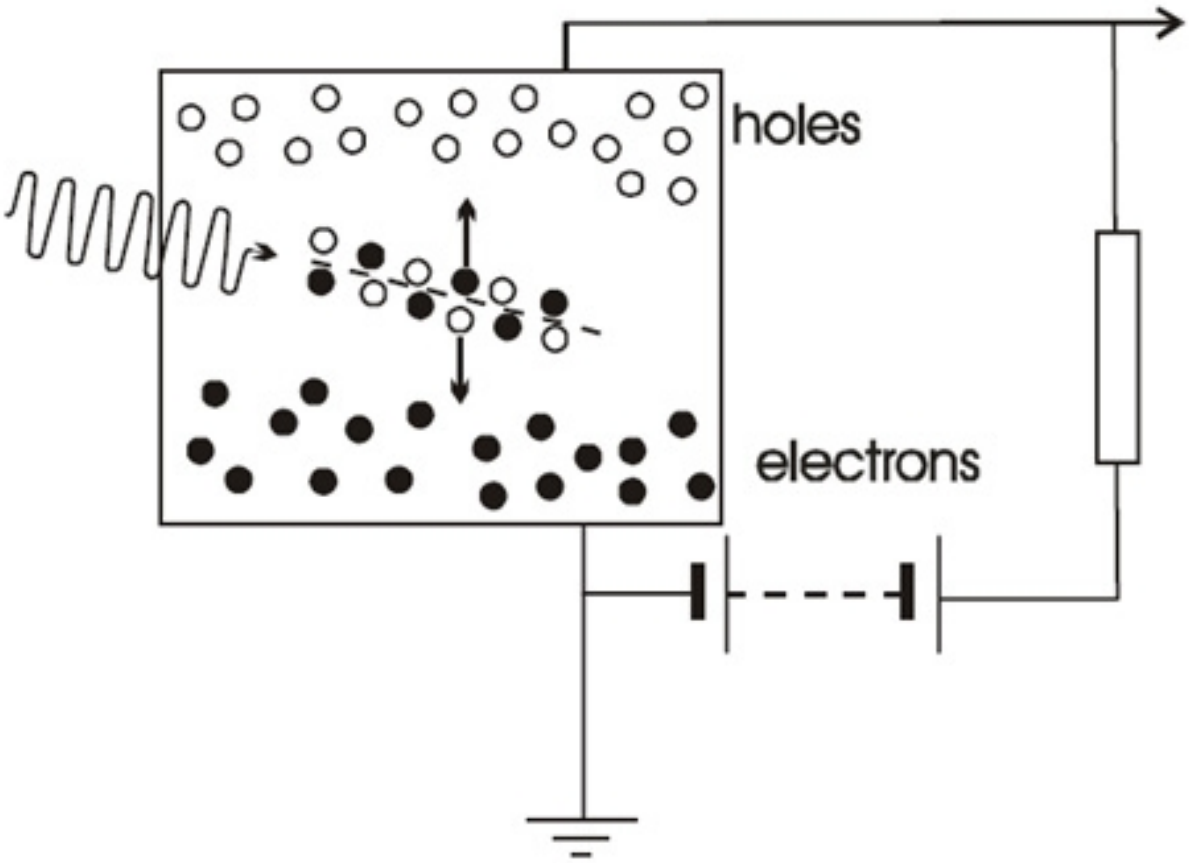
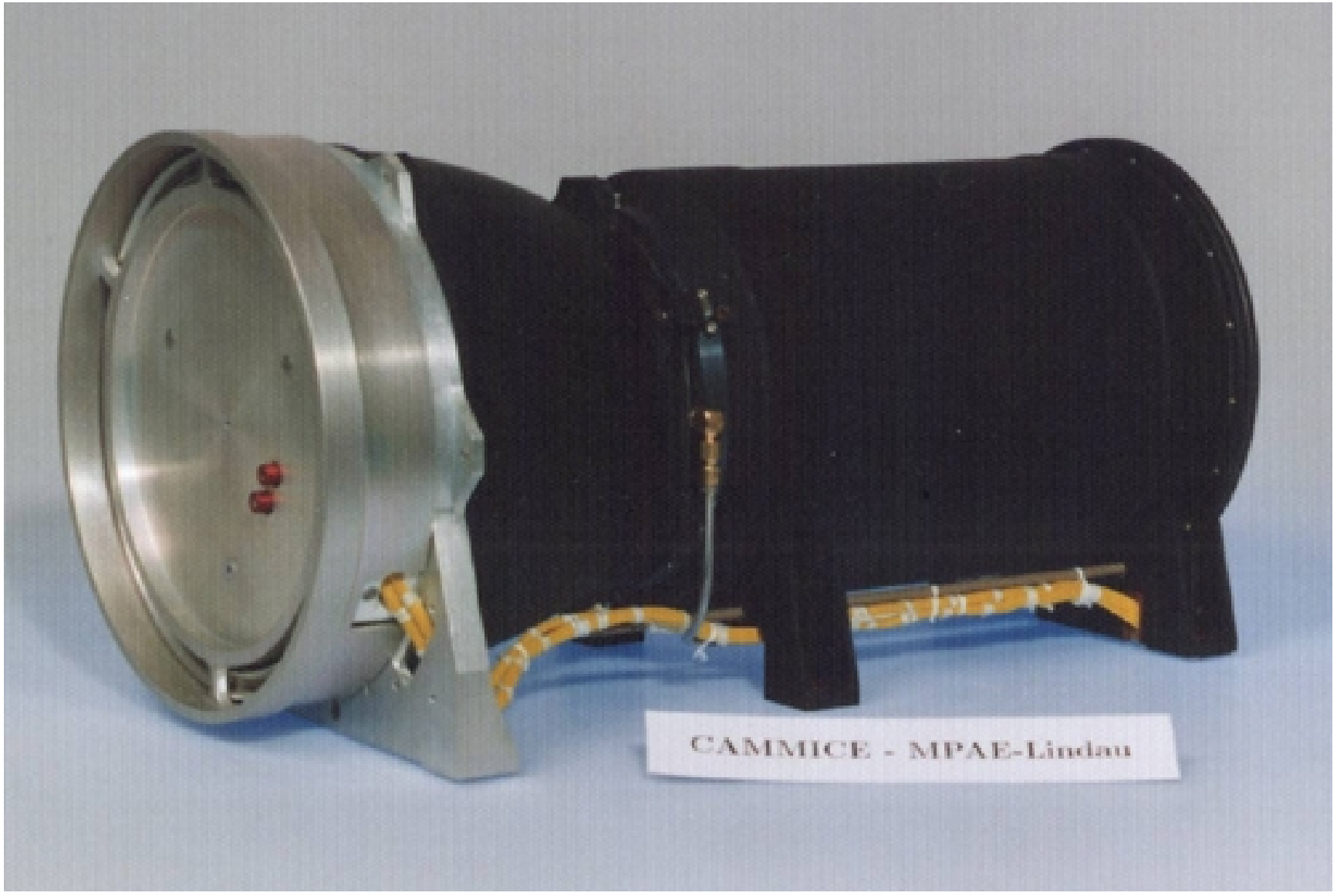
Particle Instruments

EE 521 Spring 2012 Lecture 13

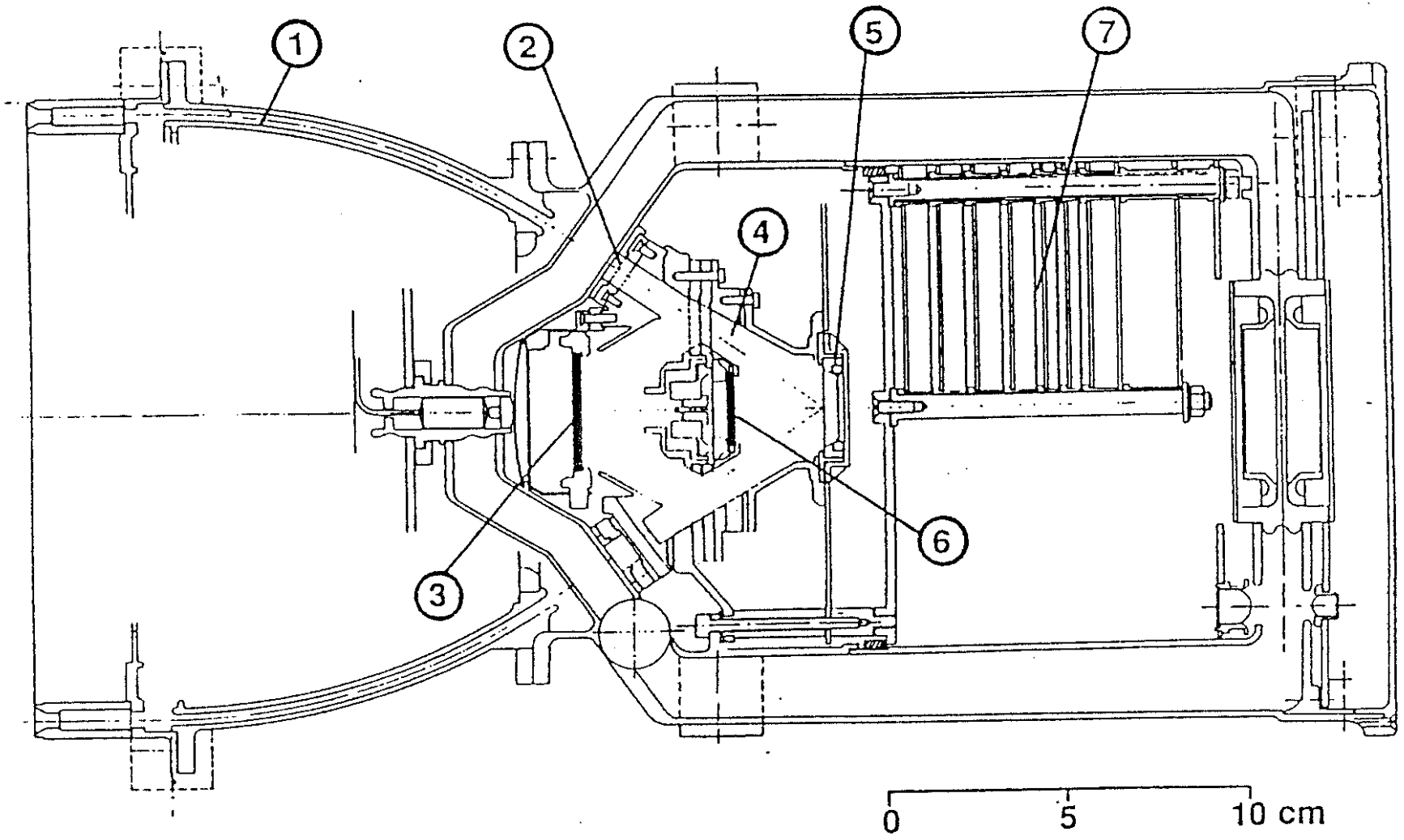
Semiconductor Detectors



Magnetospheric Ion Composition Sensor (MICS) on the Polar Satellite



MICS on the Polar Satellite



MICS Electrostatic Analyzer

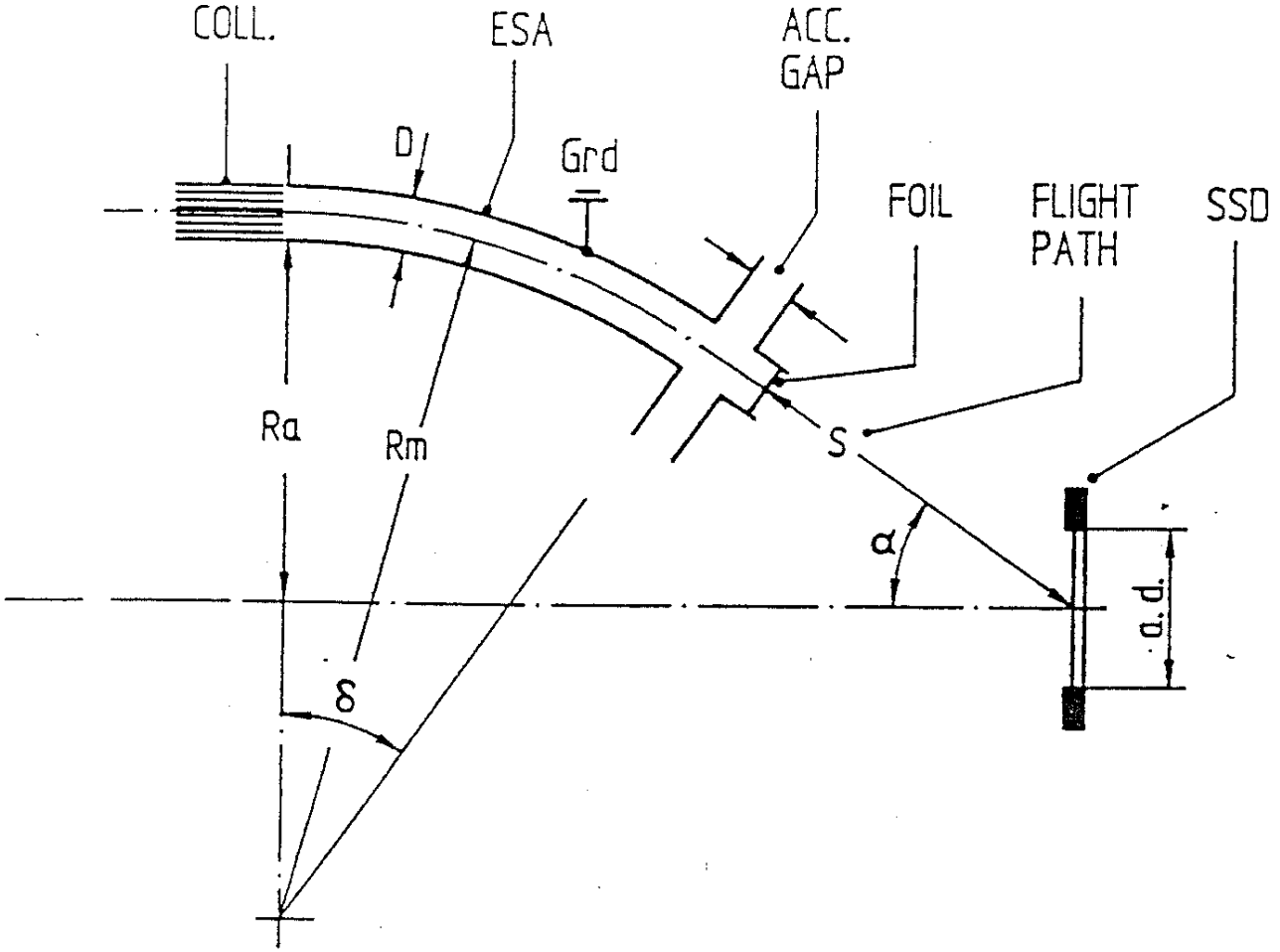


Fig. 1.2 Schematic representation of the ion path in MICS. There are two high voltage regions: The electrostatic analyzer (ESA) and the the post acceleration potential (ACC GAP). Secondary electrons are generated at the 5 $\mu g/cm^2$ thick foil and at the solid state detector (SSD).

MICS Functional Block Diagram

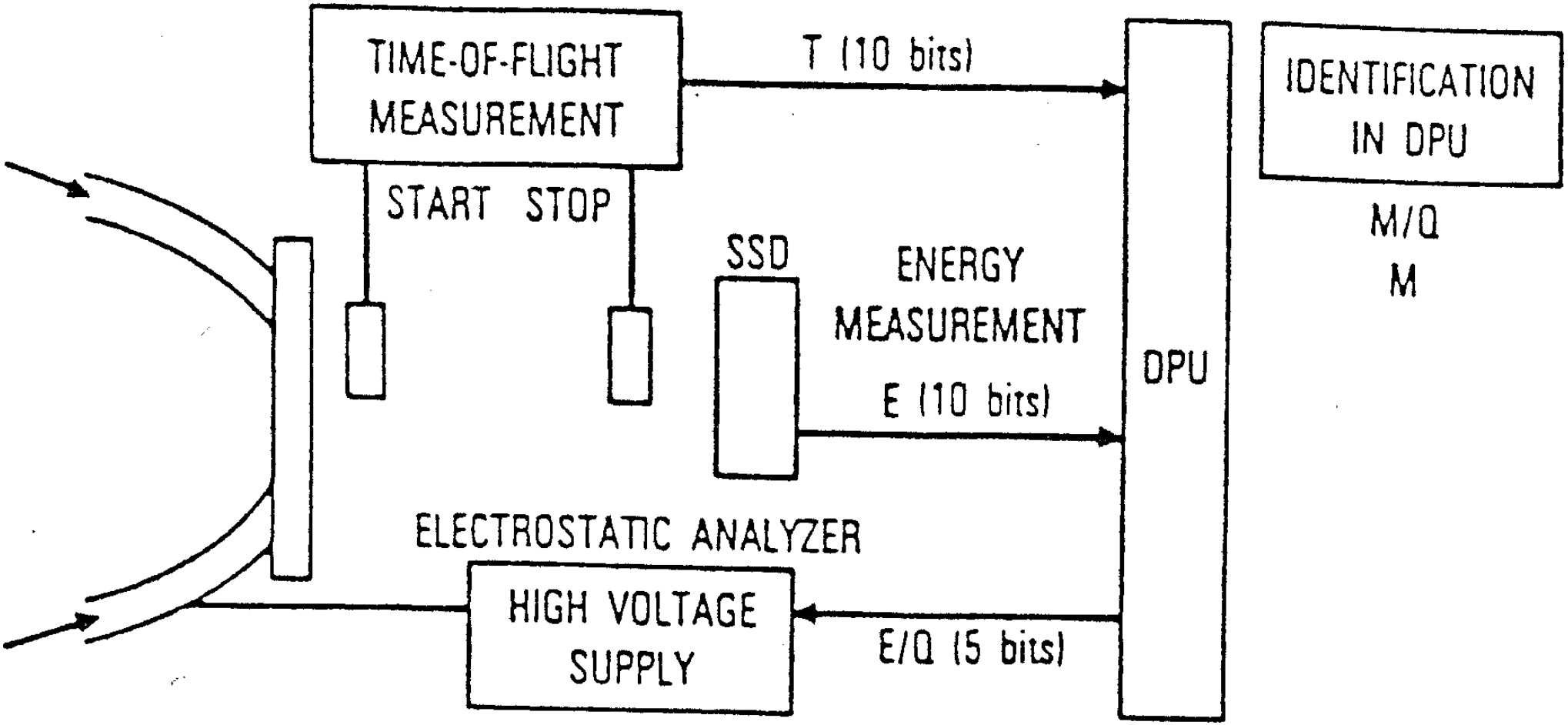
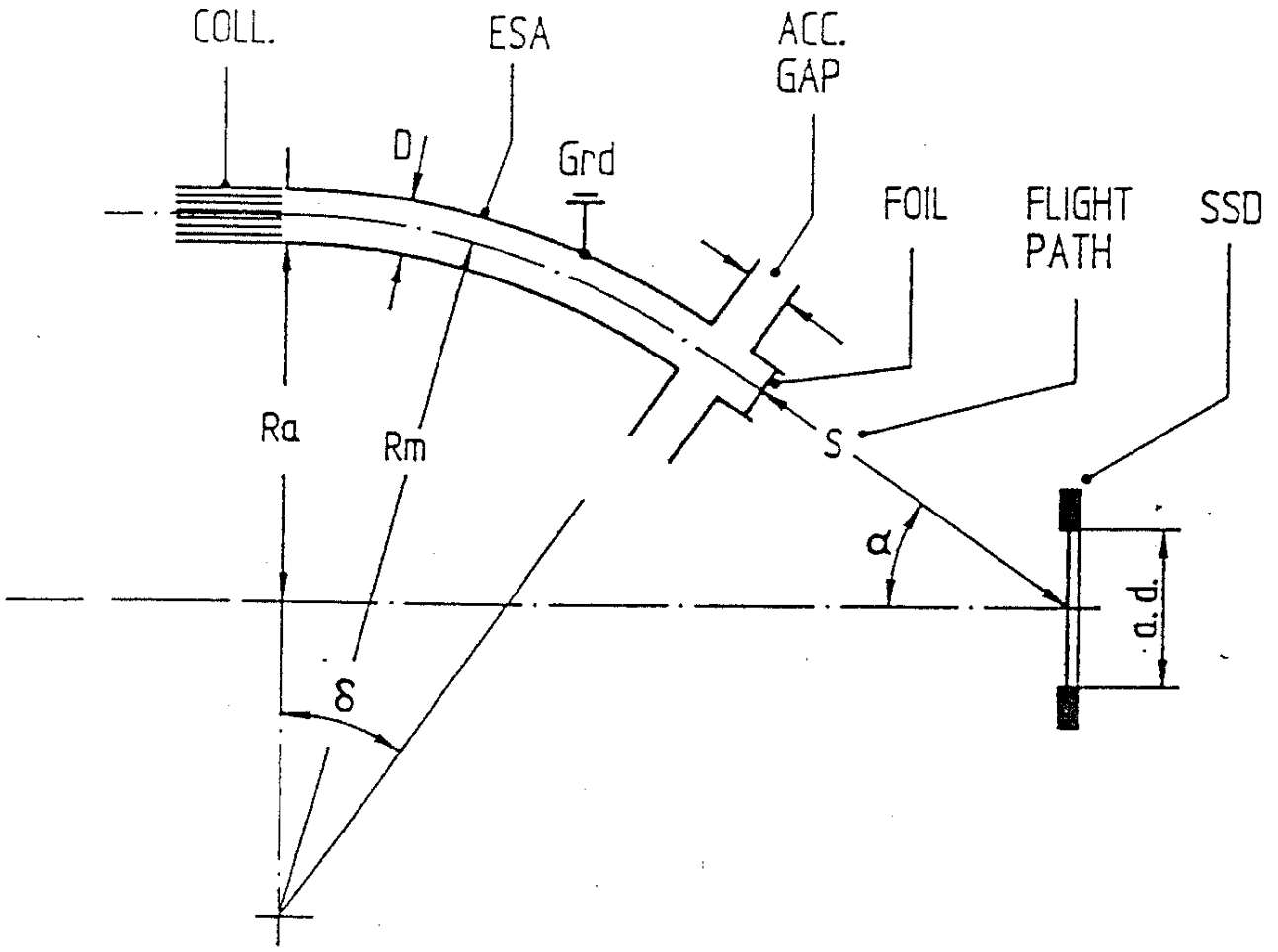


Fig. 1.5 MICS functional block diagram.

MICS Electrostatic Analyzer



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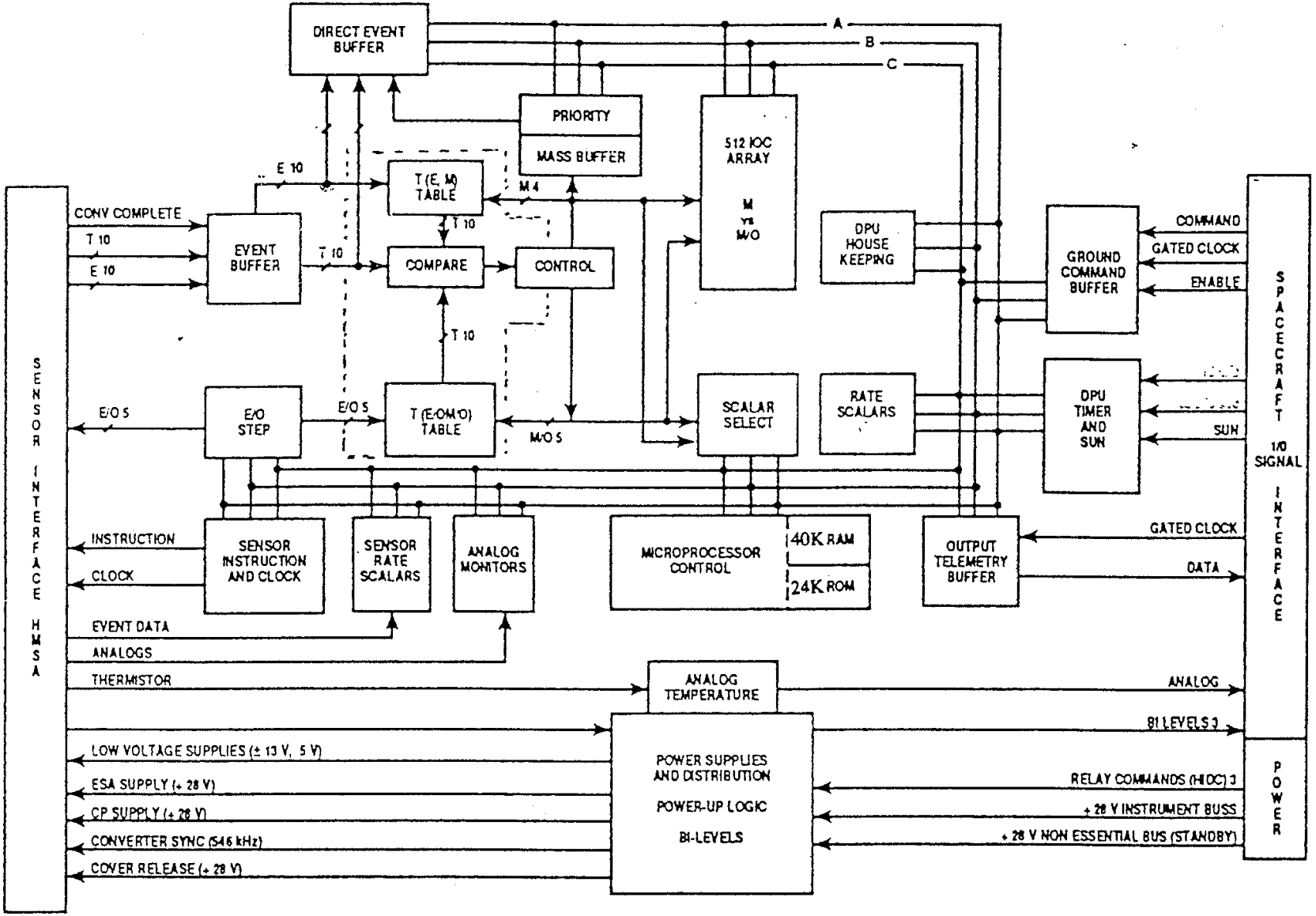
MICS Hardware Overview

1.2.1 MDPU Hardware Overview

MDPU consists of a computer, peripheral sections such as various I/O buffers and the Event Processor, the power supply, and the analog signal handler, as shown in Fig. 1.6. The computer is made up of a microprocessor (Sandia 1802), control logic (programmed in Actel A1020 FPGAs), and memory (24K bytes of PROM and 40K bytes of RAM), all biased at 5.0V. The radiation-hardened 1802 microprocessor operates with a 1.6 MHz clock. The MDPU software is stored in power-strobed 8Kx8 PROMs (Raytheon R29793SM) from the highly power consuming T^2L logic family because of the difficulty in obtaining radiation-hardened low-power PROMs. Shortly after MDPU is turned on, the contents of the PROMs are copied to low-power RAMs (IBM 6408TRH) and thereafter the software executes exclusively in RAM (the PROMs are fully powered only during infrequent accesses by the software). The 1802 microprocessor has a 64K address space: locations $0000 – $3FFF and $C000 – $DFFF are assigned to PROM ($ indicates hex); $4000 – $7BFF and $E000 – $FBFF are assigned to "software" RAM; and the remainder of the address space is allocated to MDPU's Event Processor ("hardware RAM"). This memory allocation scheme is summarized in Table 1.3.

MICS MDPU


DIRECT EVENT BUFFER
A
B
C
PRIORITY
MASS BUFFER
512 IOC ARRAY
M vs M/O
E 10
T (E, M) TABLE
M 4
T 10
CONV COMPLETE
T 10
E 10
EVENT BUFFER
T 10
COMPARE
CONTROL
T 10
DPU HOUSE KEEPING
GROUND COMMAND BUFFER
COMMAND
GATED CLOCK
ENABLE
SPACECRAFT I/O SIGNAL INTERFACE
E/O S
E/O STEP
E/O S
T (E/O/M/O) TABLE
M/O S
SCALAR SELECT
RATE SCALARS
DPU TIMER AND SUN
SUN
SENSOR INTERFACE HMSA
INSTRUCTION
CLOCK
SENSOR INSTRUCTION AND CLOCK
SENSOR RATE SCALARS
ANALOG MONITORS
MICROPROCESSOR CONTROL
40K RAM
24K ROM
OUTPUT TELEMETRY BUFFER
GATED CLOCK
DATA
EVENT DATA
ANALOGS
THERMISTOR
ANALOG TEMPERATURE
ANALOG
BI LEVELS 3
LOW VOLTAGE SUPPLIES (± 13 V, 5 V)
ESA SUPPLY (+ 28 V)
CP SUPPLY (+ 28 V)
CONVERTER SYNC (546 kHz)
COVER RELEASE (+ 28 V)
POWER SUPPLIES AND DISTRIBUTION
POWER-UP LOGIC
BI-LEVELS
RELAY COMMANDS (HIDC) 3
+ 28 V INSTRUMENT BUSS
+ 28 V NON ESSENTIAL BUS (STANDBY)
POWER