Lecture 2 - E

Analog Signal Conditioning

EE 521: Instrumentation and Measurements

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2 - E.1

Contents

2 - E.2

1 Sampling

Nyquist Sampling Theorem

- Theoretically, to avoid aliasing a continuous signal must be sampled at least twice the maximum frequency.
- Just twice the maximum frequency requires ideal filters, therefore in practice need to sample more than twice the maximum frequency.
- Use antialiasing filter to avoid aliasing. Investigate the specification of the antialiasing filter present in the device to determine the proper sampling frequency.

2 - E.3

2 Quantization

Source of Quantization Error

- In order to represent digital signals, after sampling the continuous signal must be quantized to a finite number of bits resulting in *quantization error*.
- Given a maximum peak-to-peak voltage V_{max}, the step size Δ between levels is given by

$$\Delta = \frac{V_{max}}{2^n - 1} \tag{1}$$

where n is the number of bits and $q = 2^n$ is the number of levels.

2 - E.4

Signal-to-Quantization Ratio

The ith sample after quantization my be expressed as

$$m_{\delta_q}(t) = m(t_i) + \varepsilon(t_i) \tag{2}$$

The signal-to-quantization ratio is defined as

$$(SNR)_Q = \frac{\overline{m^2(t)}}{\overline{\varepsilon^2(t)}} \tag{3}$$

and assuming the quantization error is uniform

$$\frac{-1}{2}\Delta \leq \varepsilon(t_i) \leq \frac{1}{2}\Delta \tag{4}$$

therefore, and assuming $m(t)$ is uniform,

$$(SNR)_Q = 12\frac{\overline{m^2(t)}}{\Delta^2} = 2^{2n} \tag{5}$$

2 - E.5

Word-Error Probability

$$P_w = 1 - (1 - P_b)^n \tag{6}$$

where P_b is the bit-error probability and P_w is the word-error probability. The effect of word error is in the range of

$$\frac{-1}{2}q\Delta \leq \varepsilon_w \leq \frac{1}{2}q\Delta \tag{7}$$

Assuming ε_w is uniform

$$\overline{\varepsilon_w^2} = \frac{1}{12}q^2\Delta \tag{8}$$

Further, the noise power can be written as

$$N = \overline{\varepsilon^2}(1 - P_w) + \overline{\varepsilon_w^2}P_w \tag{9}$$

where the first half of the equation above is due to quantization error and the second half is due to word error. Therefore,

$$(SNR)_D = \frac{\frac{1}{12}q^2\Delta}{\frac{1}{12}\Delta^2(1 - P_w) + \frac{1}{12}q^2\Delta^2 P_w} \tag{10}$$

Assuming P_w is negligible

$$(SNR)_D = 2^{2n} \tag{11}$$

which in dB is

$$10\log_{10}(SNR)_D = 6.02n \tag{12}$$

Hence, every bit added increases $(SNR)_D$ by 6.02 dB. 2 - E.6

Dithering

Dithering a method to statistically reduce quantization errors and harmonic distortion in analog-to-digital converters. This is achieved by adding a signal uncorrelated with the input before sampling. This signal may be a broadband noise in the signal bandwidth or a narrowband noise close to the Nyquist frequency.

2 - E.7

3 Digital-to-Analog Converter

DAC Types

- R-2R resistor ladder network.
- Binary weighted.
- Oversampling DACs.

See Figure 1. 2 - E.8

R-2R ladder network

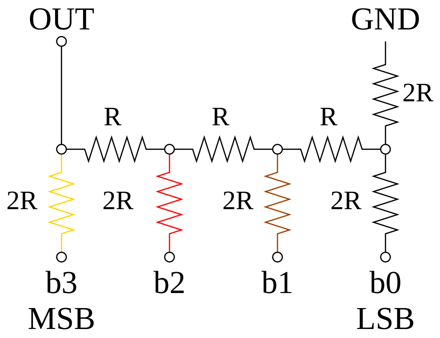


Figure 1: 4-bit R2R resistor ladder

Simple, straight forward but slow. 2 - E.9

Binary Weighted

See Figure 2.

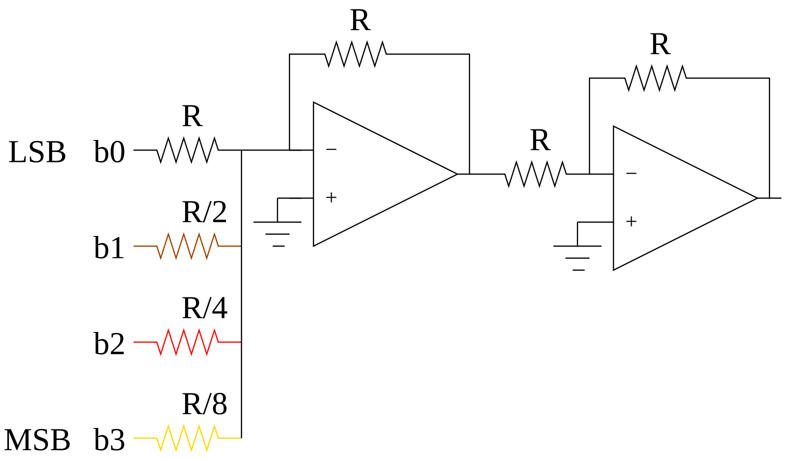


Figure 2: 4-bit binary weighted converter

Fast but requires high precision components. 2 - E.10

Oversampling DAC

See Figure 3. 2 - E.11

4 Analog-to-Digital Converter

ADC Types

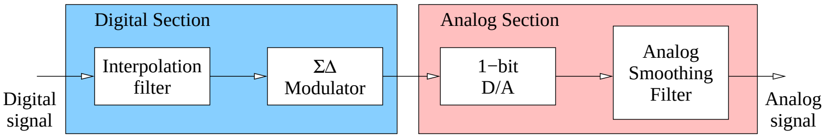


Figure 3: Elements of an oversampling DAC

- Successive approximation.
- Dual slope, integrating converters.
- Sigma-Delta converters.
- Flash converters.

2 - E.12

Successive Approximation

1. Works by comparing a the signal to different quantization levels.
2. Low cost and moderate complexity.
3. Accuracies ranging 8-16 bits.
4. Fast enough for audio signals.

2 - E.13

Dual Slope

1. Works by ramping up a signal linearly. A counter is used to to measure the time required to reach the input signal.
2. Accuracies up to 22-bits.
3. Slow conversion time.
4. High frequency noise rejection.

2 - E.14

Sigma-Delta ADC

See Figure 4.

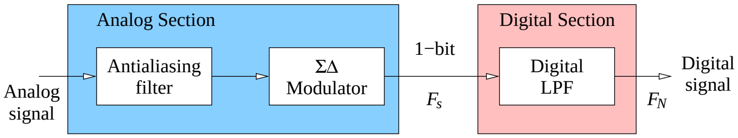


Figure 4: Elements of an oversampling ADC

2 - E.15

Flash ADCs

See Figure 5

1. Very fast but requires more power.
2. Limited in resolution since for every additional bit the number of comparators is doubled.

2 - E.16

Trade-offs

See Figure 6. 2 - E.17

5 Sigma Delta Modulation

Overview

See Figure 7. 2 - E.18

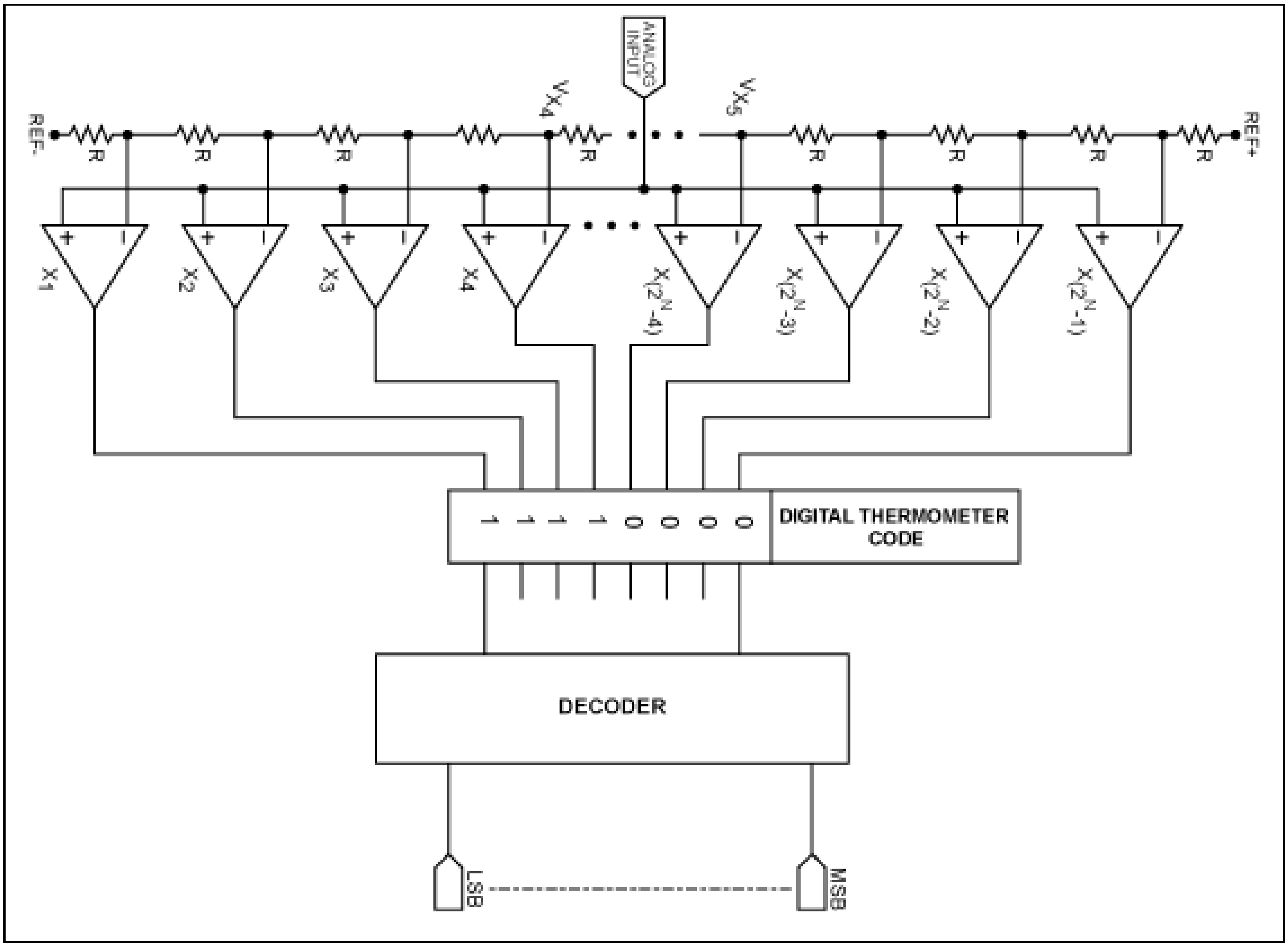
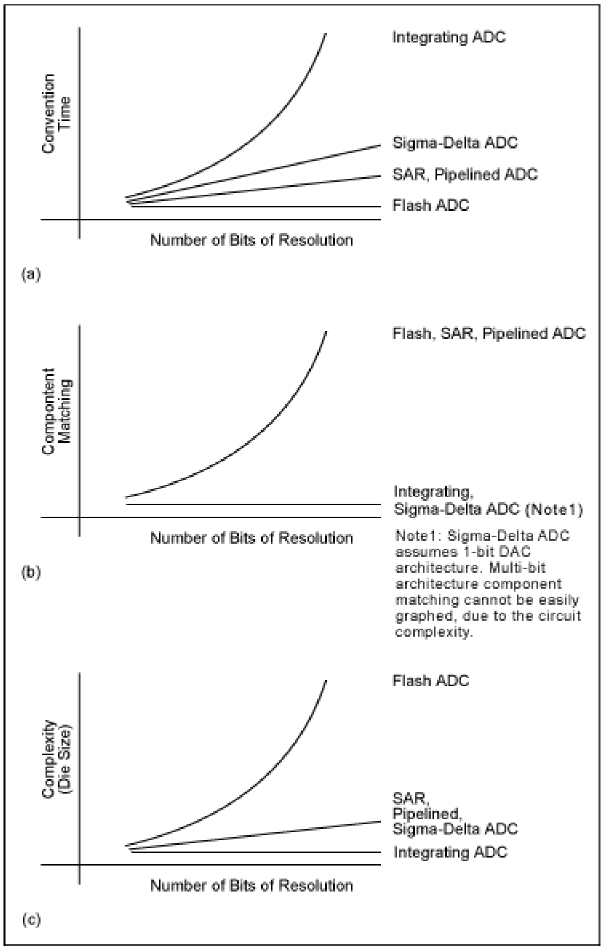


Figure 5: Flash ADC



Note1: Sigma-Delta ADC assumes 1-bit DAC architecture. Multi-bit architecture component matching cannot be easily graphed, due to the circuit complexity.

Figure 6: Trade-offs

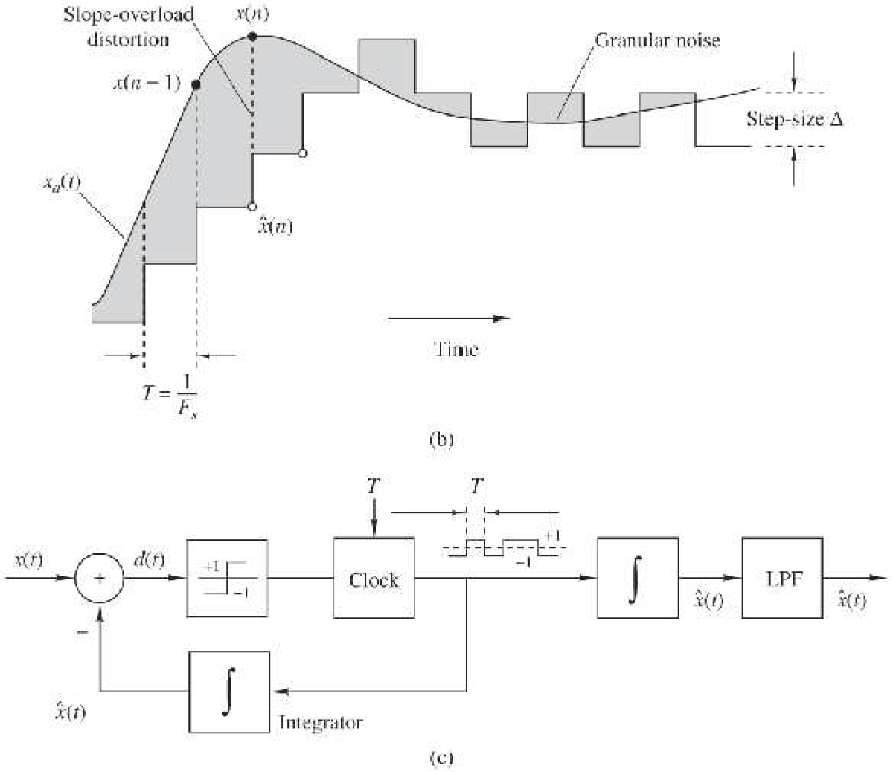


Figure 7: ©J.G. Proakis and D.G. Moanolakis, *Digital Signal Processing*, 4th Edition, Prentice Hall, 2007