Lab 11
Using a Ripple Counter to Provide a Sequence of Logic Input Combinations

Prelab

In this experiment we will build a three-bit majority circuit. This is a circuit whose output is high if the majority of its inputs are high. Therefore, the system should output a high signal if two or more of the three inputs are high.

1. Read the instructions for the lab exercise so you understand the purpuse of this prelab.
2. Construct a truth table for the circuit described above.
3. Use a K-map to reduce the resulting function.
4. Draw a fully-labeled circuit schematic from the reduced equation using only chip types 7408, 7404, and 7432. See lab 8 instructions for pin-out diagrams of these devices.

Lab Exercises

Since this ripple counter will cycle through all the truth table values in order, it will provide, in sequence, all of the possible input combinations to our system. So we connect the counter circuit to our majority circuit and it will essentially drive itself. The least significant bit (LSB) on the counter is $Q1$ and the LSB on our circuit is input C so they will be connected to each other. Likewise, $Q2$ will be paired with B, and $Q3$ will be paired with A. So, we will use the first three outputs of the ripple counter $Q3$, $Q2$, and $Q1$ as the inputs A, B, and C to our three-bit majority circuit.

As a sequential logic component, the 4040 counter requires a TTL clock input to drive and govern the speed of its counting. We will use the TTL feature on the function generator built in to the protoboard. This will be connected to the clock input on the counter. The 4040 also requires connections to Vcc and ground. It has an additional input called Reset which forces all outputs low. This input is an active high port, which means you connect Vcc to engage the reset. Remember that you must connect it to ground to disengage the reset. (As with all logic devices "no connection" is not the same as "zero" or "low.") We will connect the reset to a logic switch so we can reset on command to restart counting at 000.

The resulting output of the system can be observed on a logic probe which will detect the HI/LO state of what it is touching, indicating the state with an LED and audible tone. As the output sequences through its

values, the logic probe will play a 'song'. We can speed up or slow down the TTL clock input to control the tempo. We will watch and listen for the output pattern 'song' defined by the timing diagram we generated in the lab introduction lecture.

Finally, we will connect your circuit to a logic analyzer which can plot the inputs and outputs over time, generating a timing diagram that documents its actual behavior.

Building the Majority Circuit

Start your experiment by building the majority circuit you designed in the prelab.

1. Be sure you have the correct truth table before you begin.
2. As you will need to access the inputs easily for various purposes, dedicate a bus on your protoboard to each input A, B, and C.
3. Connect the F, output to a place on your board that you can identify and access easily for testing. It might even be a good idea to connect it to one of the logic tester ports on the protoboard, but we will still use a logic probe.

Connecting the Ripple Counter

1. Wire up your counter (74HC4040) as described in the pre-lab lecture
   - The Clock input of the counter chip will be driven by the TTL clock on the protoboard. Connect the Clock input on the 4040 to a TTL output port on the protoboard (do not connect to the ports for various shaped waveforms).
   - Select the top range switches to Hz and 10, then you can slide the 0.1-1 slider to adjust the frequency.
   - Just to be safe, be sure to adjust the amplitude slider to 5v or so (this function only applies to the other waveform shapes, but in case you connected to one of those instead of the TTL port you'd blow your circuit if the amplitude here were adjusted over 5v.)
   - Connect the Reset input to a logic switch at the bottom of the board so we can control whether it is connected to Vcc or Ground, thus turning on and off the reset function.
2. Connect the counter to the majority circuit
   - The $Q1$-$Q3$ outputs of the counter chip will be hooked up as inputs to the majority circuit, so they will be connected to the buses you created for A, B, and C.
   - Be sure to get the bit order correct, matching LSB to LSB and MSB to MSB.

Testing the System

1. Use the logic probe to test your circuit by sampling the F, output.
2. If you slow the protoboard clock enough so that you can hear the transitions, you should be able to match the sequence of lights and tones to the timing diagram output "song" you expected.

3. Call one of the lab TA's over to look over your wiring and confirm your working circuit. TA INITIALS HERE _____.

Using the Logic Analyzer to Generate a Timing Diagram

Now you need to use a logic analyzer to visually confirm the timing diagram for your circuit. Take your chip out of the socket and bring it to the protoboard connected to the logic analyzer testing station.

1. In LA Viewer you will see 16 channels on the left (0-15) where each one corresponds to a colored wire coming out of the logic analyzer. In our case, we are only using 4 channels (Ch-0...Ch-03) for A, B, C and F. We should get rid of all remaining channels by holding control to select multiple channels with the mouse, highlight all channels except the ones we are using. Press delete or right-click on the selected and choose 'delete label'.

2. To the upper right of the program you will see a clock speed in Hertz, this is how fast the program is going to sample the input, so you want this speed to be much faster than the protoboard clock. A good speed for each is 1kHzfor the protoboard and 10kHzfor LA viewer.

3. When the clock speeds are set at the desired values, acquire the signal by clicking the "play" icon. Your data should appear on the screen. Depending on your clock speeds, you may need to zoom in or zoom out (using the magnifying glass) to clearly see about two cycles through the truth table combinations on A, B and C. An easy way to check your values is to slide the blue marker at the top of the window over a transition period of the timing diagram and check to make sure that the blue numbers on the left match your truth table.

4. When you are finished with the logic analyzer timing diagram, print a copy for your lab book. The simplest way to do this is to print an application screen shot.

5. Paste the waveform printout into your lab book and describe the results.