EE 308: Microcontrollers

AVR Architecture

Aly El-Osery

Electrical Engineering Department
New Mexico Institute of Mining and Technology
Socorro, New Mexico, USA

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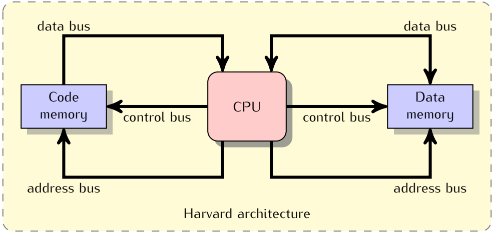
Harvard Architecture overview



- Separate buses for accessing code and data
- Faster
- Less delays
- Requires more hardware

- Data lines carry information in and out of the CPU. More lines results in faster data transfer but more complex and more expensive.
- Address lines identifies the devices and memory to be connected to the CPU
- Control lines control devices' signals for read/write as directed by the CPU

Data bus

- Carries data to and from RAM, ROM, and other devices
- More data lines facilitates more data being transferred at a time but results in more complex and expensive CPU
- Data buses are bidirectional

- Number of address lines determines the number of locations that can be addressed
- Address buses are unidirectional
- For n lines there are 2^n locations (e.g., memory) that can be addressed
- For example, 16 address lines can provide $2^{16} = 65,536$ addressable memory, i.e., 64KB?

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- 1KB = 1024 Bytes

Control bus

- Select operations of the Arithmetic Logic Unit (ALU)
- Selects read/write for the memory

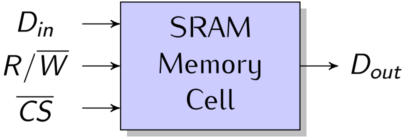
- Register file: embedded in the CPU for fast operations
- Code memory: ROM typically flash
- Data memory: RAM typically SRAM

Classification of memory

1. Volatile
   - Content is lost when power is switched off
   - Known as RAM (Random Access Memory)
   - Could be static (SRAM) or dynamic (DRAM)
2. Non-Volatile
   - Retains content even when no power is provided
   - Known as ROM (Read Only Memory)
   - Different types: ROM, PROM, EPROM, EEPROM, FLASH

SRAM

- Made of flipflops
- Requires 6 transistors each
- Each cell holds only 1 bit
- Using address decoders, how many address lines are needed to address 16Kbits memory?



- Requires only one transistor per bit
- Information is stored in a capacitor
- Less silicon area is needed
- Can achieve more memory per a given area
- Needs refreshing due to leakage
- Slower than SRAM but cheaper
- Uses multiplexers/demultiplexers to cut the required address lines in half

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Non-volatile memory

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- Electrically EPROM (EEPROM): Similar to EPROM but has charge pumps provided on the chip instead of UV. Good for about 100,000 cycles.
- Flash: Similar to EEPROM but memory is erased in blocks. Used for storing code. It is cheaper but good for around 10,000 cycles.

- Separate memory addressing: need to address each memory, SRAM, FLASH, or EEPROM separately
- Single memory range: map different memory into a single memory range

Little endian vs. big endian

Given a 16-bit value, for example 0xB60F, it is desired to save it into memory location 0x100 one byte at a time which byte gets written in the high byte and which one gets written in the low byte

- Little endian: used by most microcontrollers including AVR and Intel microprocessors

	High Byte	Low Byte
0x100	B6	0F

- Big endian: used by Freescale

	High Byte	Low Byte
0x100	0F	B6

Addressing modes

- Immediate (single-register): operand is a register and may have a constant value as a second operand, e.g.,

```
NEG   R18        ;negate the content of R18
LDI   R19,0x06   ;load 0x06 into R19
```

- Register: two registers hold the data to be manipulated

```
ADD   R20,R23    ;add R23 to R20 and store the result in R20
```

- Direct: operand is a memory location

```
LDS   R19,0x560  ;load R19 with the content of mem loc 0x560
STS   0x40,R19   ;store R19 to data space location 0x40
```

- Register indirect: operand is a register but it points to the memory location

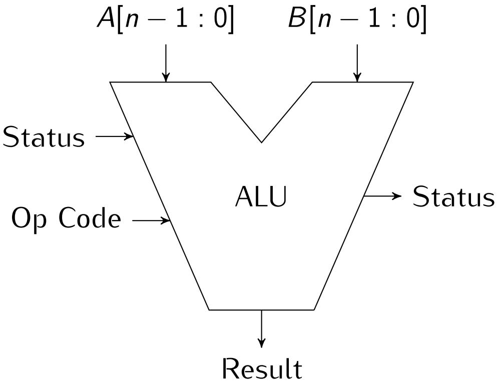
```
LDI   XL,0x30    ;load R26 (low byte of X) with 0x30
LDI   XH,0x01    ;load R27 (high byte of X) with 0x01
LD    R18,X      ;load R18 with content of memory 0x130
```

- Auto-increment/auto-decrement: content of register is pre- or post- incremented/decremented after/before memory access

```
LD    Rn,X+     ;load Rn with content pointed to by X then inc X
LD    Rn,-X     ;decrement X then load Rn by contented pointed to by new X
```

Arithmetic Logic Unit (ALU)

- Takes two inputs
- Performs arithmetic and logic operations



Status register

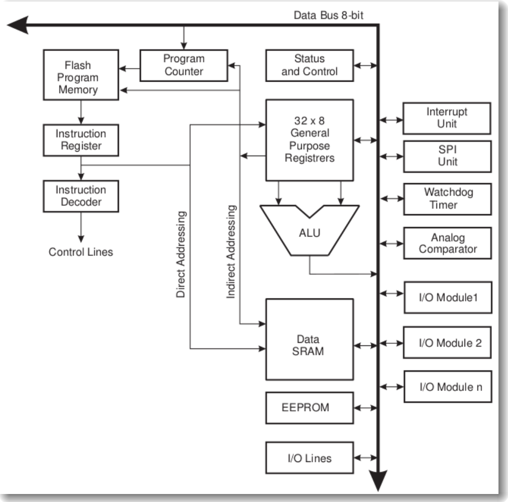
8-bit register used by the ALU to indicate arithmetic conditions

Bit	7	6	5	4	3	2	1	0	
0x3F (0x5F)	**I**	**T**	**H**	**S**	**V**	**N**	**Z**	**C**	**SREG**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	Global Interrupt Enable	Bit Copy Storage	Half Carry	Sign Flag	Overflow Flag	Negative Flag	Zero Flag	Carry Flag	

Control unit, program counter, stack and stack pointer

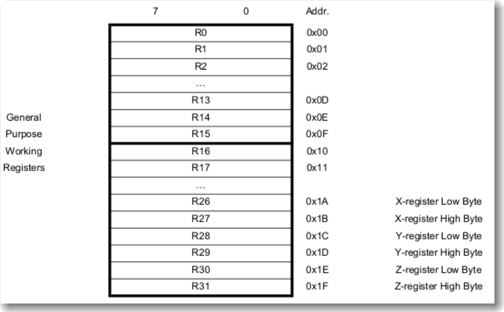
- Control unit: controls devices, data path and determines which instruction to be executed
- Program counter: address of the next instruction to be executed
- Stack: memory used by the CPU to keep track of return addresses and register contents when branching, servicing an interrupt or executing a subroutine
- Stack pointer: points to the current position in the stack

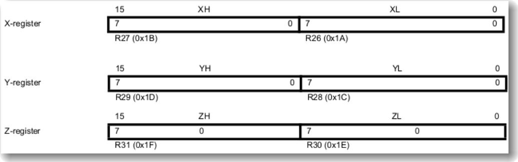
- RISC with Harvard architecture
- Code ROM
- Data RAM
- Data EEPROM
- Timers
- I/O ports
- ADC
- PWM
- Communication interfaces: USART, SPI, I2C (TWI), CAN, USB



General purpose registers

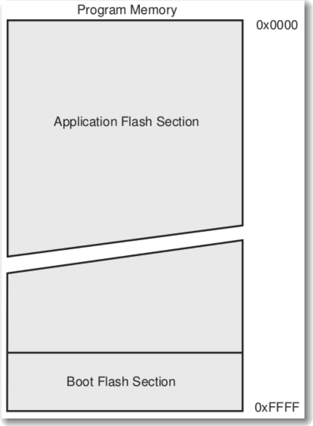
- Register provide fast method for processing
- The registers are 8-bit wide
- Most operations can be executed in one cycle

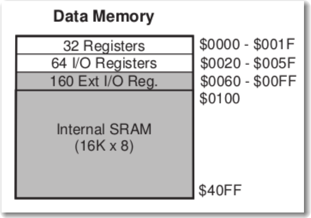




Some key specifics

- Instructions are either 2-bytes or 4-bytes
- Data lines to the data memory are 8-bit
- Data lines to the program memory are 16-bit
- Stack pointer is 16-bit


Program Memory
0x0000
Application Flash Section
Boot Flash Section
0xFFFF


Data Memory
32 Registers
64 I/O Registers
160 Ext I/O Reg.
Internal SRAM
(16K x 8)
$0000 - $001F
$0020 - $005F
$0060 - $00FF
$0100
$40FF

- I/Os and peripherals are placed in I/O space
- I/O addresses are offset from memory address by 0x20
- I/O registers in the range 0x00 to 0x1F are directly bit accessible
- IN and OUT commands must use addresses in the range 0x00 to 0x3F
- When using LD and ST commands I/O registers are addressed as data space and therefore 0x20 must be added to their addresses

- RISC architecture
- 131 instructions (most executes in single clock cycle)
- 128K bytes code ROM
- 4K bytes EEPROM
- 16K bytes SRAM
- JTAG
- Timers/counters, PWM, 8-channel 10bit ADC
- Watchdog timer
- USART, SPI, I2C