EE 231L Lab 4

Prelab Part 1

1. Read Section 3.8.8 of the Text, which discusses tri-state buffers. What does a tri-state buffer do?

2. The final circuit for the computer (Figures 2 & 3 of the lab overview) uses two tri-state buffer. The right-hand buffer is enabled when OUTPUT_ENA is active. Under what conditions will this tri-state buffer be enabled? (What is the state of the signals ADDR = 0xFF, RESET, EXT_R, EXT_W, STORE, and READ?)

3. Under what conditions will the left-hand buffer be enabled? (What is the state of the signals ADDR = 0xFF, RESET, EXT_R, EXT_W, STORE, and READ?)

4. Write the Verilog program to implement the multiplexer.

5. Write the Verilog program to implement the decoder.