EE 231 Lab 1

HCMOS Logic Family

In this lab you will get a hands-on experience designing simple logic circuits using standard integrated circuits (ICs). You will learn about timing and its effect on the circuit output.

1. Prelab

1. Write the truth table for an *inverter* gate.
2. Write the truth table for an *xor* gate.
3. Write the truth table for a *and* gate.
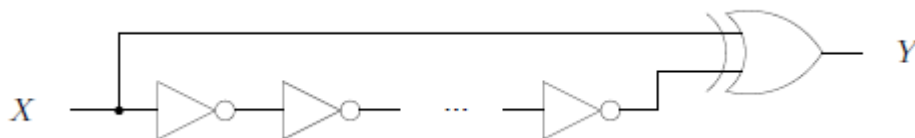4. Write the truth table for the circuit shown in Figure 1.

Figure 1. A simple circuit

2. Lab

2.1 Basic Behavior of HCMOS Logic Family

1. Use the datasheet to connect a 7404 IC.
2. Verify the operation of an inverter by connecting the input to Vcc and GND.
3. Use a variable 10kΩ pot to vary the input to the inverter, as shown in Figure 2. When does the input change?
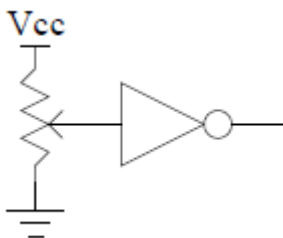

Figure 2. Changing the input to the inverter

4. Build the circuit shown in Figure 1 using 10 inverters in series. Set the output of the function generator that you built in Lab 0 to 15kHz and connect it to the input of your circuit. Can you observe the output of your circuit by using a voltmeter or

a logic probe?
5. Connect the output of your circuit to the logic analyzer and record your observations. (Use the information provided in section 3 to run the logic analyzer).
6. Does the output match what you expected? Why or why not?
7. What is the propagation delay of an inverter gate?

3. Half Adder
1. Write the truth table for the circuit shown in Figure 3.
2. Connect ICs from the 7400 IC to implement the circuit shown above.
3. Verify that operation of the circuit by connecting the inputs to different combinations of Vcc and GND.
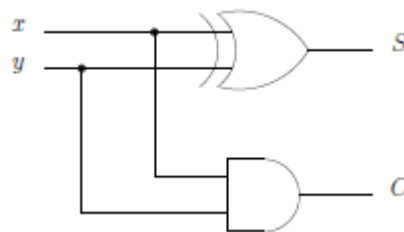4. In terms of binary arithmetic, what do the S and C outputs represent?

Figure 3. Half Adder Circuit

4. Supplementary Material

4.1 Logic Analyzer

Start the logic analyzer by double-clicking on the LA Viewer icon on the Windows desktop. Do the following:

1. From the Clock menu in the upper right corner of the LA Viewer window set the internal clock for a 5 MHz sampling rate.
2. Right-click in the left most column of the viewing area and select delete all labels.
3. Right-click in the left most column of the viewing area and select add label. Add representative names and select the appropriate channels.
4. Click on the button with a single running man. The logic analyzer will sample the logic levels on lines 0 and 1.
5. Observe the Waveform window. You can use the Magnifying Glass icons on the menu bar to zoom in and out. Does the waveform make sense to you? Print a sample of the waveform, and put it in your lab notebook. To print a copy of this waveform, make sure the logic analyzer software is in the foreground (it is the current program). Then, press Alt+PrintScrn to take a snapshot of that window. You can now paste this image into Word which will make it easy to print out.
6. Another way of displaying logic data is as numbers. Right-click on the leftmost column, select combine labels, give this label any name, move all labels from source

box to destination box where output is at the top, and the is at the bottom and click OK. Right click on that name, select Configure Labels, and change Group Type to binary. How does this numeric data compare to a truth table format?