EE 231 Prelab 2

Decoders and Multiplexers

Decoders and multiplexers are important combinational circuits in many logic designs. Decoders convert *n* inputs to a maximum of unique 2^n outputs. A special case is the binary coded decimal (BCD)-to-seven-segment decoder, where a four-bit decimal digit (represented in BCD) is decoded into the corresponding seven-segment code used as an input to the seven-segment display (Figure 1).

A simple computer has several main blocks, e.g.:

- Arithmetic Logic Unit (ALU): performs arithmetic operations on numbers.
- Memory: where the program is stored.
- Multiplexers: select which piece of information to be passed on.
- Decoders: to determine, based on the input, whether to read from memory or input/output lines.
- Computer Control Unit: outputs the control signals that direct the operation of the rest of the computer.

Even though we are not building a computer, this information give you some perspective on the different components that you will be building and what they may be used for.

In this lab we will focus on the multiplexer that chooses either a reset address (RST_ADDR), program counter (PC), memory address register (MAR), or index register X (IRX). These signals are used to determine the information required to enter the arithmetic logic unit (ALU) component of the computer.

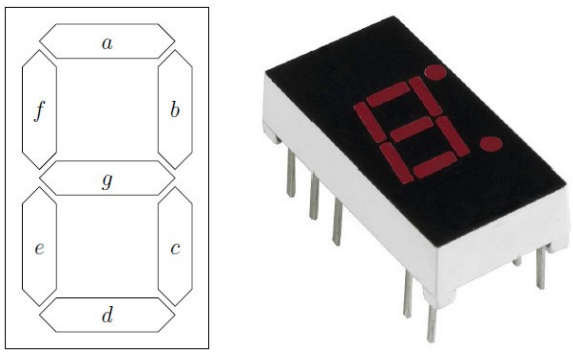

Figure 1: 7-Segment Display

1.Prelab

1.1.Connect the two 7-segment displays along with the pin header needed on a perf board.

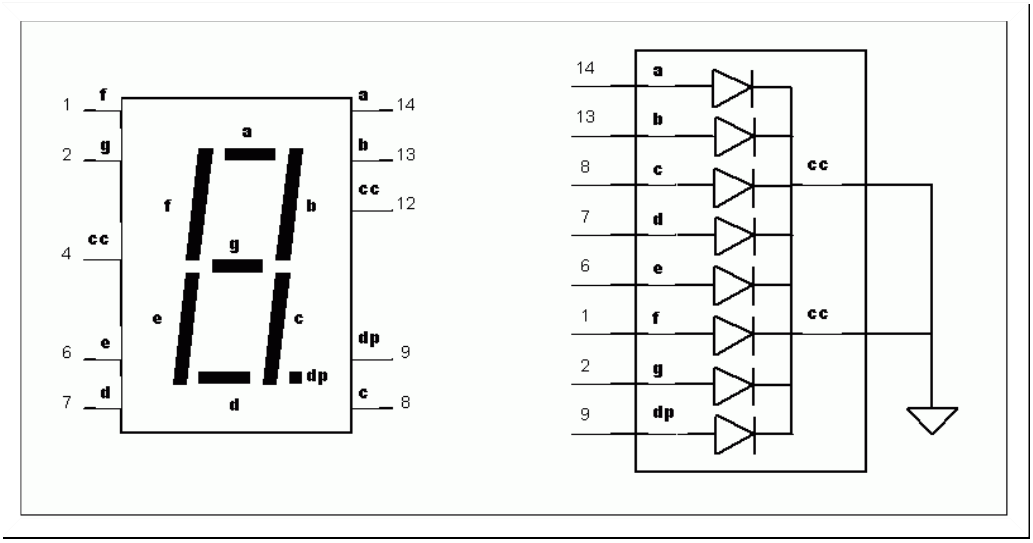

Figure 2: MAN74 7-segment display

1.2.Fill in the truth table for the BCD-to-7-segment decoder shown in Table 1, e.g., if the input is 0011, LEDs a, b, c, d, and g should be on while LEDs f and e will be off (see Figure 1 for reference). For inputs 0xA through 0xF, naturally they don't correspond to any number in the 0-9 range, therefore output the corresponding hex value instead, i.e., for 0xA the display should show the letter A.

Digit	Binary	a	b	c	d	e	f	g
0	0000							
1	0001							
2	0010							
3	0011	1	1	1	1	0	0	1
4	0100							
5	0101							
6	0110							
7	0111							
8	1000							
9	1001							
A	1010							
B	1011							
C	1100							
D	1101							
E	1110							
F	1111							

Table 1: Truth Table for 7-Segment-Display Decoder
("1" LED is on, and "0" it is off)

1.3.Design a multiplexer with ADDR_SEL as the select signal, RST_ADDR (we will use address 0xFF), P, MAR, and X as 8-bit input signals.
1.4.Design a Verilog program to implement the multiplexer/decoder from the table below.

Digit	Binary	a	b	c	d	e	f	g
0	0000							
1	0001							
2	0010							
3	0011	1	1	1	1	0	0	1
4	0100							
5	0101							
6	0110							
7	0111							
8	1000							
9	1001							
A	1010							
B	1011							
C	1100							
D	1101							
E	1110							
F	1111							

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