EE 231 Prelab 3

Adder/Subtractor

In this lab you will learn how to write several modules and instantiate them. To demonstrate this process you will design a 4-bit full adder/subtractor.

1. Prelab

1.1. Write the truth table for a full adder.

1.2. Write the truth table for a full subtractor.

1.3. Show how you can use half adders to build a full adder.

1.4. Figure 1 shows how to implement a ripple adder using a sequence of 1-bit full adders. Using an example, verify that this circuit functions as a 4-bit adder.

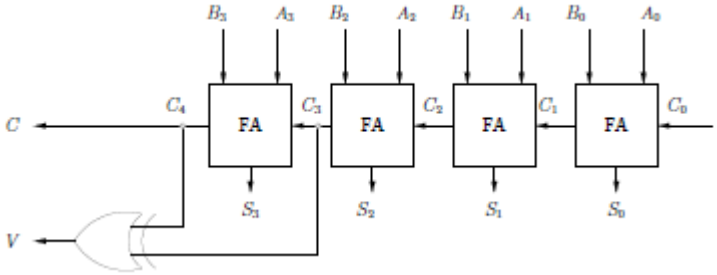

Figure 1: 4-bit Adder

1.5. **What does the V signal, which may be computed as V = C3 ⊕ C4, represent?** In order to answer this question try to use examples when you are adding two positive numbers and another when you are adding two negative numbers.

1.6. By slightly modifying the circuit shown in Figure 1 we can design an adder/subtractor as shown in Figure 2. **Why does this circuit make an adder when the sel = 0, and why does it behave as a subtractor when the sel = 1?**

1.7. Fill in Table 1.

sel	Input B	Output D in terms of B
0	$B_3B_2B_1B_0$	
1	$B_3B_2B_1B_0$	

Table 1: Outputs of an adder/subtractor

1.8. Using Table 1, write a Verilog program to implement a decoder that selects the proper input to the full adder depending on the *sel* signal.

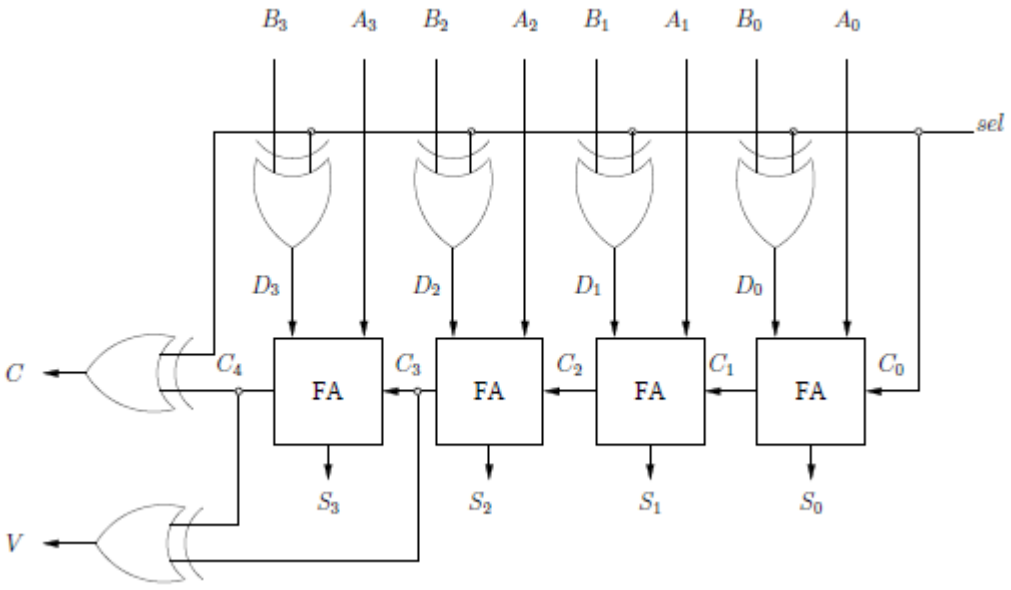

Figure 2: 4-bit Adder/Subtractor.