

## Homework #4 Due October 17, 2007

7.1 Consider the timing diagram in Figure P7.1. Assuming that the D and Clock inputs shown are applied to the circuit in Figure 7.12, draw the waveforms for the  $Q_a$ ,  $Q_b$ ,  $Q_c$  signals.

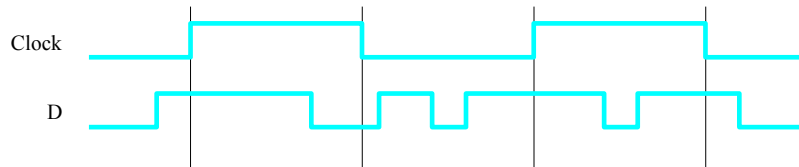
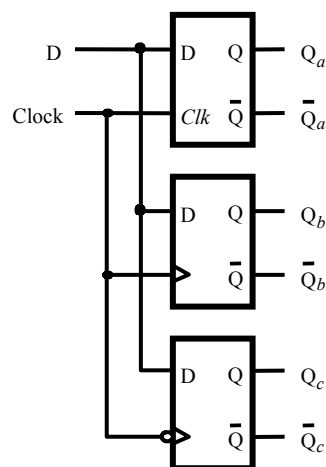


Figure P7.1. Timing diagram for problem 7.1.



(a) Circuit

Figure 7.12. Comparison of level-sensitive and edge-triggered D storage elements.

7.5 Given a 100-MHz clock signal, derive a circuit using D FF to generate 50-MHz and 25-MHz clock signals. Draw a timing diagram for all three clock signals, assuming reasonable delays.

7.6 An SR FF is a FF that has set and reset input like a gated SR latch. Show how an SR FF can be constructed using a D FF and other logic gates.

7.13 A universal shift register can shift in both the left-to-right and the right-to-left directions, and it has a parallel-load capability. Draw a circuit for such a shift register.

7.20 Construct a NOR-gate circuit, similar to the one in Figure 7.11a, which implements a negative-edge-triggered D FF.

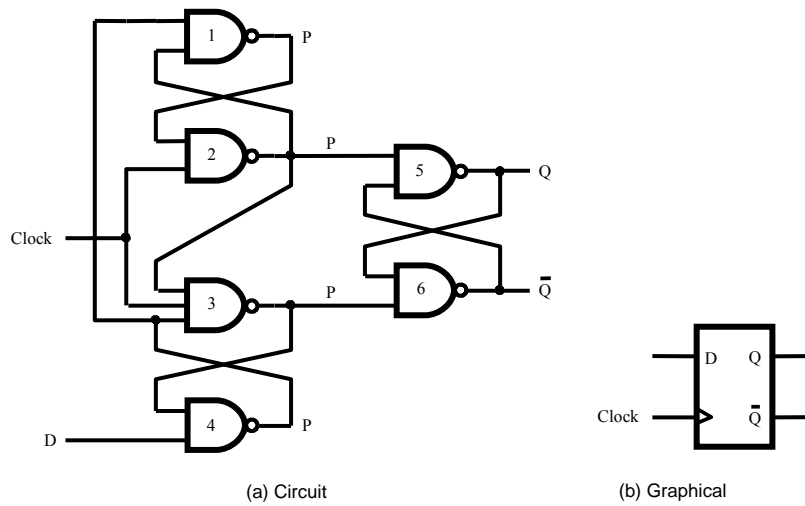


Figure 7.11. A positive-edge-triggered D flip-flop.

7.30 A ring oscillator is a circuit that has an odd number,  $n$ , of inverters connected in a ringlike structure, as shown in Figure P7.5. The output of each inverter is a periodic signal with a certain period.

(a) Assume that all the inverters are identical; hence they all have the same delay, called  $t_p$ . Let the output of one of the inverters be named  $f$ . Give an equation that expresses the period of the signal  $f$  in terms of  $n$  and  $t_p$ .

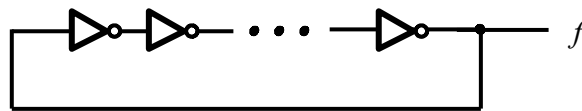


Figure P7.5. A ring oscillator.

(b) For this part you are to design a circuit that can be used to experimentally measure the delay  $t_p$  through one of the inverters in the ring oscillator. Assume the existence of an input called Reset and another called Interval. The timing of these two signals is shown in Figure P7.6. The length of time for which Interval has the value 1 is known. Assume that this length of time is 100 ns. Design a circuit that uses Reset and Interval signals and the signal  $f$  from part (a) to experimentally measure  $t_p$ . In your design you may use logic gates and sub circuits such as adders, flip-flops, counters, registers, and so on.

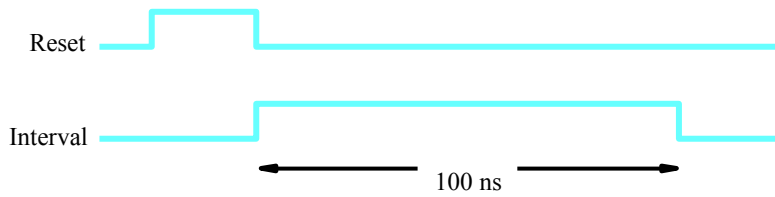


Figure P7.6. Timing of signals for problem 7.31.

7.32 A logic circuit has two inputs, Clock and Start, and two outputs,  $f$  and  $g$ . The behavior of the circuit is described by the timing diagram in Figure P7.8. When a pulse is received on the Start input, the circuit produces pulses on the  $f$  and  $g$  output as shown in the timing diagram. Design a suitable circuit using only the following components: a three bit resettable positive-edge-triggered synchronous counter and basic logic gates. For your answer assume that the delays through all logic gates and the counter are negligible.

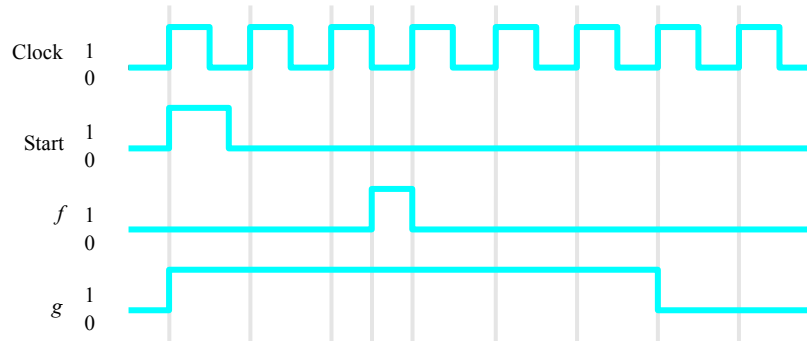


Figure P7.8. Timing diagram for problem 7.33.