EE 231 – Homework Chapter 2

2.6 Use the Venn diagram to prove that

$$(x1 + x2 + x3) \cdot (x1 + x2 + \overline{x3}) = x1 + x2$$

2.8 Draw a timing diagram for circuit in Figure 2.19a. Show the waveforms that can be observed on all wires in the circuit.

2.10 Use algebraic manipulation to show that the three input variables x1, x2, and x3

$$\sum m(1,2,3,4,5,6,7) = x1 + x2 + x3$$

2.11 Use algebraic manipulation to show that the three input variables x1, x2, and x3

$$\prod M(0,1,2,3,4,5,6) = x1x2x3$$

2.30 Design the simplest circuit that has four inputs, x1,x2, x3, and x4, which produces an output value of 1 whenever three or more of the input variables have the value 1; otherwise, the output has to be 0.

2.39 Implement the circuit in Figure 2.33 using NAND and NOR gates.

2.46 Write Verilog code to implement the circuit in Figure 2.27a using the gate level primitives.

2.49 Write Verilog code to implement the function f(x1, x2, x3)=$\sum m(0,1,3,4,5,6)$ using the continuous assignment.

$$f = \overline{x2} + \overline{x1}x3 + x1\overline{x3}$$