EE 231 – Homework Chapter 3

3.3 (a) Show that the circuit in Figure P3.3 is functionally equivalent to the circuit in Figure P3.2.

(b) How many transistors are needed to build this CMOS circuit if each XOR gate is implemented using the circuit in Figure 3.61d?

3.6 (a) Give the truth table for the CMOS circuit in Figure P3.4.

(b) Derive a canonical SOP expression for the truth table in part (a). How many transistors are needed to build a circuit representing the canonical form if only AND, OR, and NOT gates are used?

3.9 Figure P3.7 shows half of a CMOS circuit. Derive the other half that contains the NMOS transistors.

3.13 Derive a CMOS complex gate for the logic function $f = xy + xz + yz$. Use as few transistors as possible (Hint: consider $\bar{f}$).

3.21 For the circuit in Figure P3.8, assume that the values $k'n = \frac{60\mu A}{V^2}, k'p = 0.4k'n,$ $\frac{Wn}{Ln} = 0.5\frac{\mu m}{0.5\mu m}, \frac{Wp}{Lp} = \frac{4.0\mu m}{0.5\mu m}, VDD = 5V, and\ VT = 1V$. When Vx=0, calculate the following:

(a) The static current, Istat.

(b) The on-resistance of the PMOS resistor.

(c) VHO

(d) The static power dissipated in the inverter.

(e) The on –resistance of the NMOS transistor

(f) Assume that the inverter is used to drive a capacitive load of 70 fF. Using eq. 3.4, calculate the low-to-high and high-to-low propagation delays.

3.27 For a CMOS inverter, assume that the load capacitance is C=150 fF and VDD=5V. The inverter is cycled through the low and high voltage levels at an average rate of f = 75 MHz.

(a) Calculate the dynamic power dissipated in the inverter.

(b) For a chip that contains the equivalent of 250,000 inverters, calculate the total dynamic power dissipated if 20% of the gates change values at any given time.

3.44 Consider the function $f(x1, x2, x3) = x1\overline{x2} + x1x3 + x2\overline{x3}$. Show a circuit using 5 two-input lookup-tables (LUTs) to implement this expression. As shown in Fig 3.39, give the truth table implemented in each LUT. You do not need to show the wires in the FPGA.

3.50 Assume that a gate array exists in which the logic cell used is a three-input NAND gate. The inputs to each NAND gate can be connected to either 1 or 0, or to any logic signal. Show how the following logic functions can be realized in the gate array (Hint: use DeMorgan's theorem.)

a) $f = x1x2 + x3$

b) $f = x1x2x4 + x2x3\overline{x4} + \overline{x1}$