EE 231 – Homework Chapter 5

5.4 Convert to decimal numbers 73, 1906, -95, and -1630 into signed 12-bit numbers in the following representations:
(a) Sign and magnitude
(b) 1's complement
© 2's complement

5.5 Perform the following operations involving 8-bit 2's complement numbers and indicate whether arithmetic overflow occurs. Check your answers by converting to decimal sign-and-magnitude representation.

00110110	01110101	11011111
+01000101	+11011110	+10111000
00110110	01110101	11010011
-00101011	-11010110	-11101100

5.7 Show that the circuit in Figure 5.5 implements the full-adder specified in Figure 5.4a.

5.15 What is the critical delay path in the multiplier in Figure 5.3? What is the delay along this path in terms of the number of gates?

5.14 In Figure 5.18 we presented the structure of a hierarchical carry-lookahead adder. Show the complete circuit for a four-bit version of this adder, built using 2 two-bit blocks.

5.16 (a) Write a Verilog module to describe the circuit block in Figure 5.36b. Use the CAD tools to synthesize a circuit form the code and verify its functional correctness.
(b) Write a Verilog module to describe the circuit block in Figure 5.36c. Use the CAD tools to synthesize a circuit from the code and verify its function correctness.
(c) Write a Verilog module to describe the 4×4 multiplier shown in Figure 5.36a. Your code should be hierarchical and should use the subcircuits designed in parts (a) and (b). Synthesize the circuit from the code and verify its functional correctness.

5.24 Show a graphical interpretation of three-digit decimal number, similar to Figure 5.12. The left-most digit is 0 for positive numbers and 9 for negative numbers. Verify the validity of your answer by trying a few examples of addition and subtraction.