EE 231 – Homework Chapter 7

7.3 Figure 7.5 shows as latch build with NOR gates. Draw a similar latch using NAND gates. Derive its characteristic table and show its timing diagram.

7.10 Write Verilog code that represents a T flip-flop with an asynchronous clear input. Use behavioral code, rather than structural code.

7.17 Design a three-bit up/down counter using D flip-flops. It should include a control input called ~Up/Down. If ~Up/Down = 0, then the circuit should behave as an up-counter. If ~Up/Down = 1, then the circuit should behave as a down-counter.

7.21 Write Verilog code that represents a modulo-12 up-counter with synchronous reset.

7.31 A circuit for a gated D latch is shown in Figure P7.7. Assume that the propagation delay through either a NAND gate or an inverter is 1 ns. Complete the timing diagram given in the figure, which shows the signal values with 1n resolution.