

First Class August 24, 2011

Instructor:

Hector Erives; Phone: 505-835-5932; Email: erives@ee.nmt.edu

Textbook:

- Fundamentals of Digital Logic with Verilog Design, Second Edition
Stephen Brown and Zvonko Vranesic

Class Schedule

Mon, Wed, Fri 9:00 – 9:50, MSEC 103

Office Hours

Mon, Wed, Fri: 10:00-11:00 A.M., and Tue, Thurs: 9:00 - 10:00 A.M.

Course Overview:

This course develops on a basic understanding, design, and implementation of digital systems. Topics include number systems, Boolean logic, logic gates, design of combinatorial circuits, reduction of combinatorial circuits, register transfer logic, and design of complex digital systems. Synthesis, simulation and implementation of digital systems using Verilog.

Tentative Class Structure

Item	Description	Points
Homework	Homework will be assigned regularly and will be done on individual basis	10
Quizzes	Short quizzes will be given on Fridays.	10
Partial tests	Three mid-term exams.	3x20=60
Final test	Comprehensive final test	20

Laboratory information:

Check <http://www.ee.nmt.edu/~erives/classes.php> web page for more information.

Academic honesty

All students are expected to demonstrate personal integrity. Interaction among students regarding homework assignments are strongly encouraged, however each student *must show his/her individual effort*. Exchange of information during in-class examinations as well as copying homework solutions from each other is strictly prohibited. Students exhibiting any form of academic dishonesty will be subject to penalties in accordance with NMT policies.