Mini Project

Introduction

FPGAs are usually used as "glue logic" devices to interface various processor components in digital systems. Recently, FPGAs and CPLDs have been used to implement digital ADCs [1,2]. In theory, a simple ADC can be implementing using an FPGA or a CPLD using a simple RC network connected to their Low Voltage Differential Signaling (LVDS) inputs.

Digital ADC implementation on FPGAs/CPLDs

FPGAs/CPLDs, with LVDS capability, may be used to implement digital ADCs, also known as Delta-Sigma Analog-to-Digital converters. The ADC consists of a comparator (implemented by an LVDS input), a high speed 1-bit sampling register (implemented by a D flip-flop), and a low pass filter and decimation filter which may be implemented in the form of a cascaded integrator-comb (CIC) filter [3].

Materials

The objective of this miniproject is to implement an ADC. We are interested in digitizing acoustic signals so you will also need a microphone. You are required to implement, test, and demonstrate, only one ADC channel.

Because the signal coming out of the microphone is very small, you need to amplify it. Keep in mind that the voltage levels in an FPGA are 0-3.3 V. The EE department will provide funding to buy microphones and a GPS system which will be used for the final project. Adafruit and Sparkfun sell GPS boards and electret microphone boards with an amplifier already in them.

Requirements

Use the following requirements to choosing the clocking speed of the different digital components of your ADC:

Voltage range: 0-3.3 V.
Sampling frequency: 16 kHz.
Bit-resolution: 16 bits.
RC network: simple 1st. order RC, and you can check references for guidelines.

Deliverables

1. Short report (<4 pages) describing your implementation of the ADC (40%).
2. Demonstration of your ADC (60%).

Note: You must include the Verilog code and the schematics/block diagram of the circuit in your report.

References

[1] "Leveraging FPGA and CPLD Digital Logic to Implement Analog to Digital Converters," *A Lattice Semiconductor White Paper*, March 2010.
[2] Allan Chin, Luciano Zoso, "How to Implement **All-Digital** analog-to-digital converters in FPGAs and ASICs," *EE Times*, January 2011.
[3] Richard Lyions, "Understanding cascaded integrator-comp filters", *Embedded*, March, 2005.