Electrical Engineering
New Mexico Institute of Mining and Technology

EE 531 Fall 2014

Instructor:
Prof. Hector Erives; Phone: 505-835-5932; Email: erives@ee.nmt.edu.

Textbook :
Advanced Digital Design with the Verilog HDL, 2nd. Edition, Michael D. Ciletti

Software:
Verilog, C, MATLAB

Class Schedule:
MW 11:00-12:15 A.M., Workman 116

Office Hours:
M-F: 10:00-11:00 A.M.

Prerequisites
Digital Electronics (EE231) or equivalent, or consent of instructor.

Course Overview:
The objective of the course is to develop an understanding and obtain hands-on experience with the Verilog HDL, and use it to implement a dedicated embedded processor. Examine differences between synchronous and asynchronous FSMs, and design a complex system using the HDL programming language in a CAD environment.

Grading:
- Homework: 20%
- Mini-projects: 30%
- Participation: 20%
- Final project (Demonstration & Report): 30%

Note: A 30% deduction applies to late homework, demonstrations, and reports.

Topics:
- Review of Combinatorial Logic Design
- Fundamentals of Sequential Logic Design
- Introductions to Logic Design with Verilog
- Logic Design with Behavioral Models of Combinatorial and Sequential Logic
- Synthesis of Combinatorial and Sequential Logic
- Design and Synthesis of Datapath Controllers
- (Programmable Logic and Storage Devices)
- (Algorithms and Architecture for Digital Processors)