EE 231 - Homework 1

Due Oct. 3, 2016

1. Do the Prelab for *Lab 5: Registers*
   (a) Design an eight-bit synchronous latch in Verilog
   (b) Design an eight-bit PC register in Verilog
   (c) Write a program which calls the above two designs to test that they function properly
2. Problem 5.21 from textbook