1. Simulate the following Verilog programs. Use timing diagrams to show if the D flip-flops are reset **synchronous** -or-a**synchronously.**

a)

```
module flipflop (D, Clock, Resetn, Q);
        input D, Clock, Resetn;
        output reg Q;

        always @(negedge Resetn, posedge Clock)
        if (!Resetn)
                Q < = 0;
            else
                Q < = D;
endmodule
```

b)

```
module flipflop (D, Clock, Resetn, Q);
        input D, Clock, Resetn;
        output reg Q;

        always @(posedge Clock)
        if (!Resetn)
            Q < = 0;
        else
            Q < = D;
endmodule
```

2. Find out how Verilog implements (Mux or Gate) the code below.

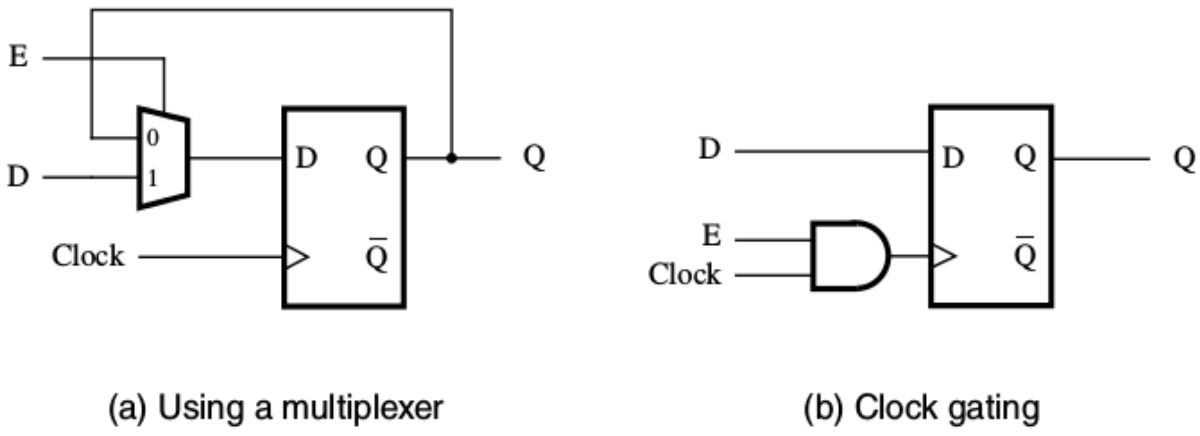

Figure 5.56 Providing an enable input for a D flip-flop.

```
module rege (D, Clock, Resetn, E, Q);
    input D, Clock, Resetn, E;
    output reg Q;

    always @(posedge Clock, negedge Resetn)
        if (Resetn == 0)
            Q <= 0;
        else if (E)
            Q <= D;

endmodule
```

Figure 5.57 Code for a D flip-flop with enable.