Due November 23, 2016

Homework 8

Name_____

Assume that the Transmitter of the figure below accepts parallel data, $\mathbf{B = b_7 , b_6 , \ldots , b_0}$, representing ASCII characters. Assume also that bit $\mathbf{b_7}$ is set to **0**. The circuit is supposed to generate a parity bit, **p**, and send it instead of $\mathbf{b_7}$ as a part of the serial transfer. The Figure below gives a possible circuit. An **FSM** is used to generate the parity bit , which is included in the output stream by using a multiplexer. A three-bit counter is used to determine when the **p** bit is transmitted, which happens when the count reaches **7**.

1. - Design the desired FSM.

2.- Design a Receiver that detects errors in one of the bits of each byte received